

Hadley17" MLK Schematics Document

Broadwell ULT

2014-10-09

REV :A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRETE OPTIMUS installed

UMA



Wistron Corporation
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Title

Cover Page

Size
A3

Document Number

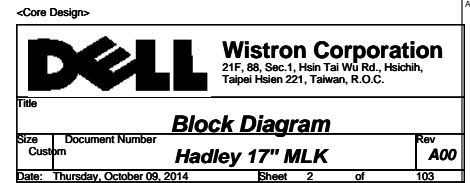
Hadley 17" MLK

Rev
A00

Date: Thursday, October 09, 2014

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Project code : 4PD02N010001
PCB P/N : DCPXP
PCB No : 14202-1



(Blanking)

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<Core Design>



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Title

(Reserved)

Size
A3

Document Number

Hadley 17" MLK

Rev

A00

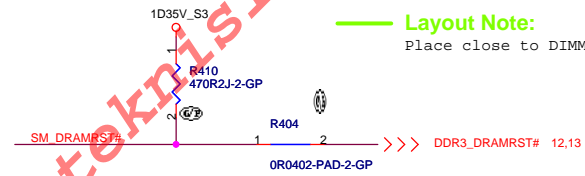
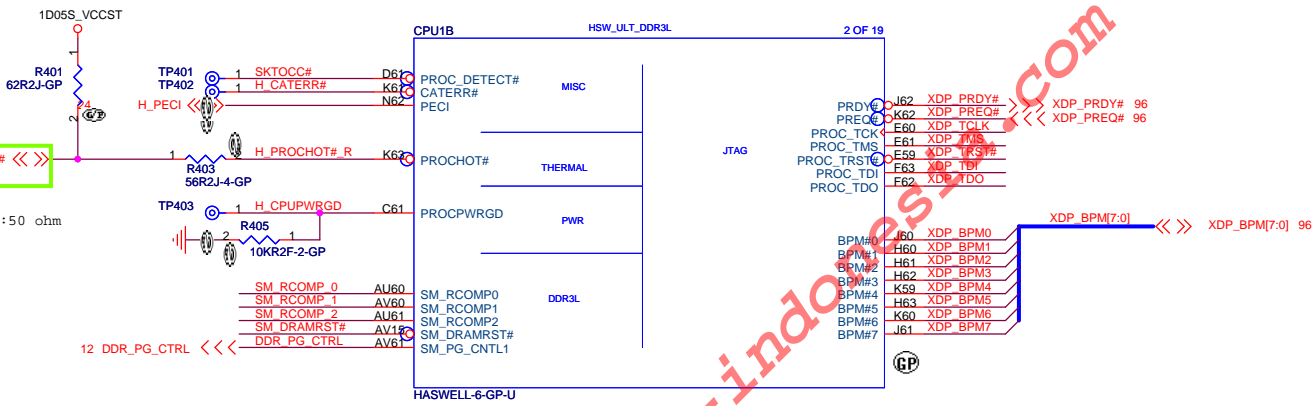
Date: Friday, September 19, 2014

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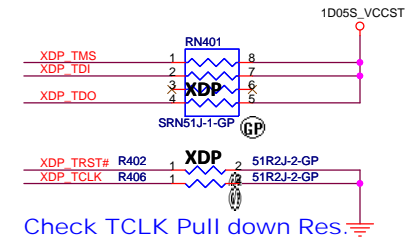
24,42,44,46 H_PROCHOT# <<>>
Layout Note:
Impedance control:50 ohm

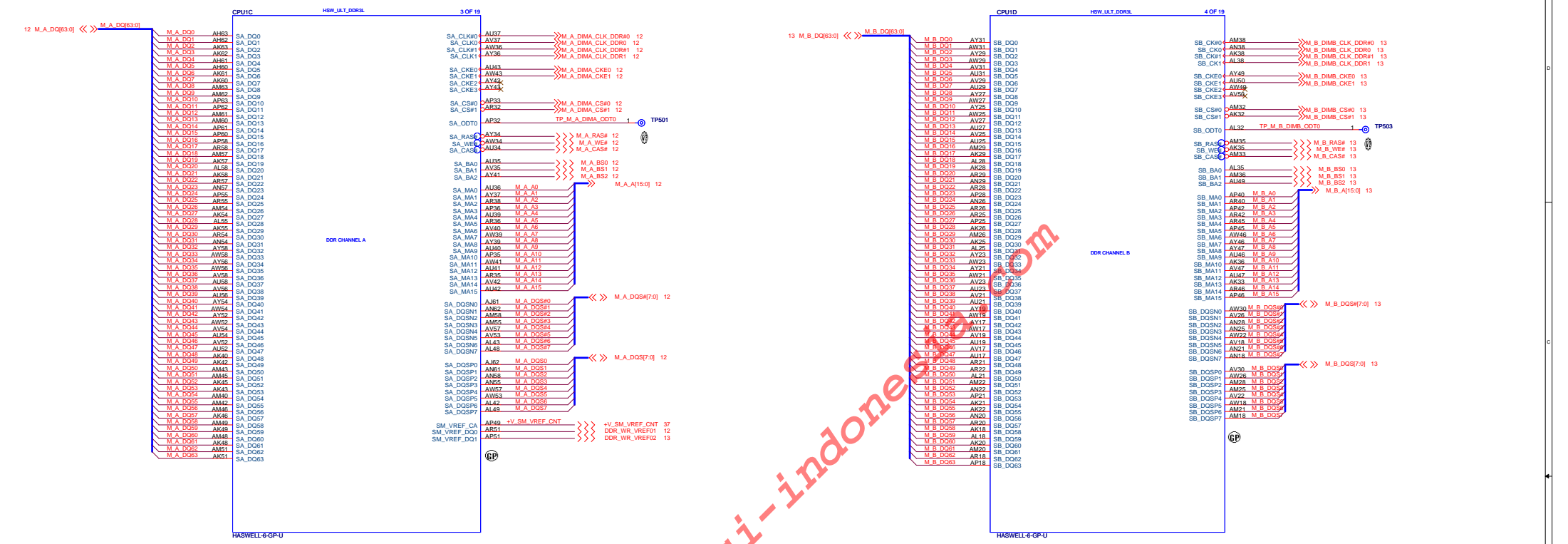


Layout Note:
Design Guideline:
SM_RCOMP keep routing length less than 500 mils.



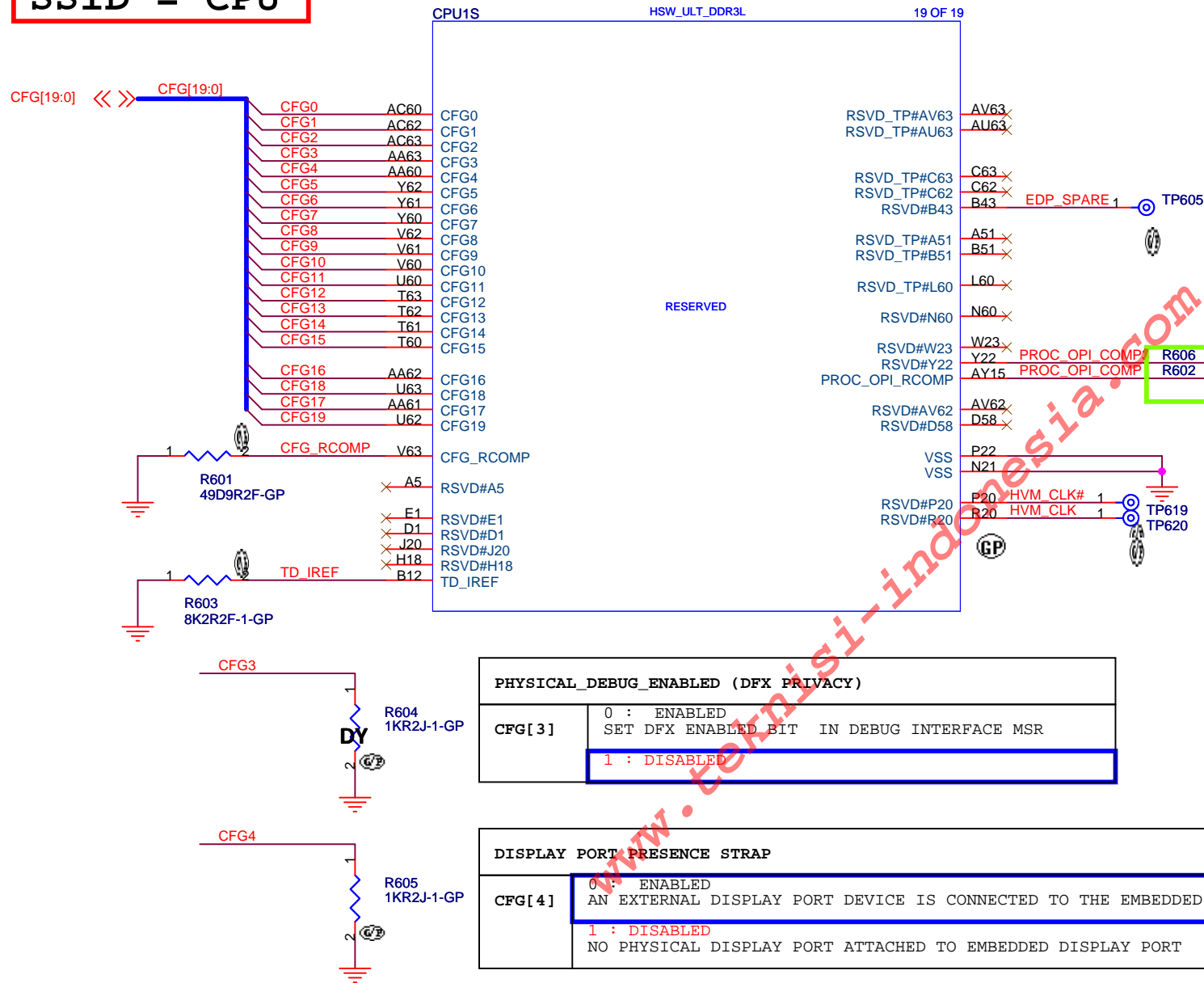
Layout Note:
Place close to DIMM





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SSID = CPU



Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

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Title

CPU (RESERVED)

Size
A4

Document Number

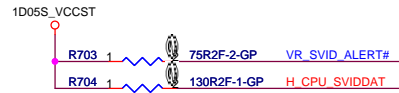
Hadley 17" MLK

Rev
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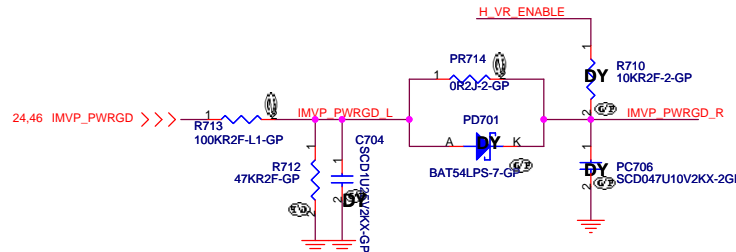
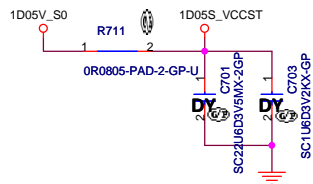
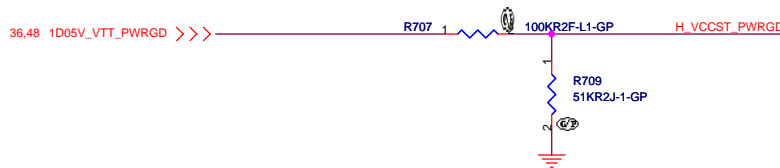
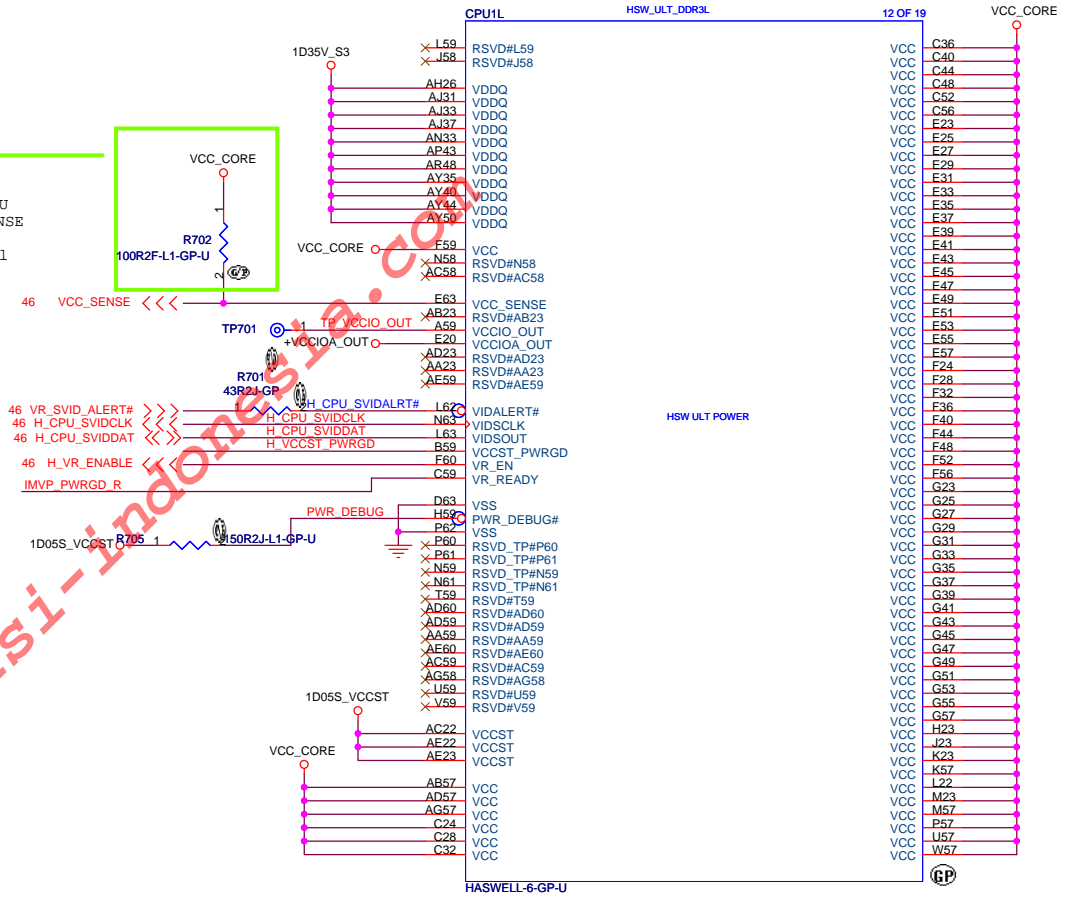
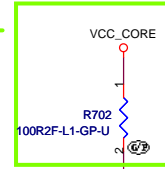
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SSID = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Lwnngth match<25mil

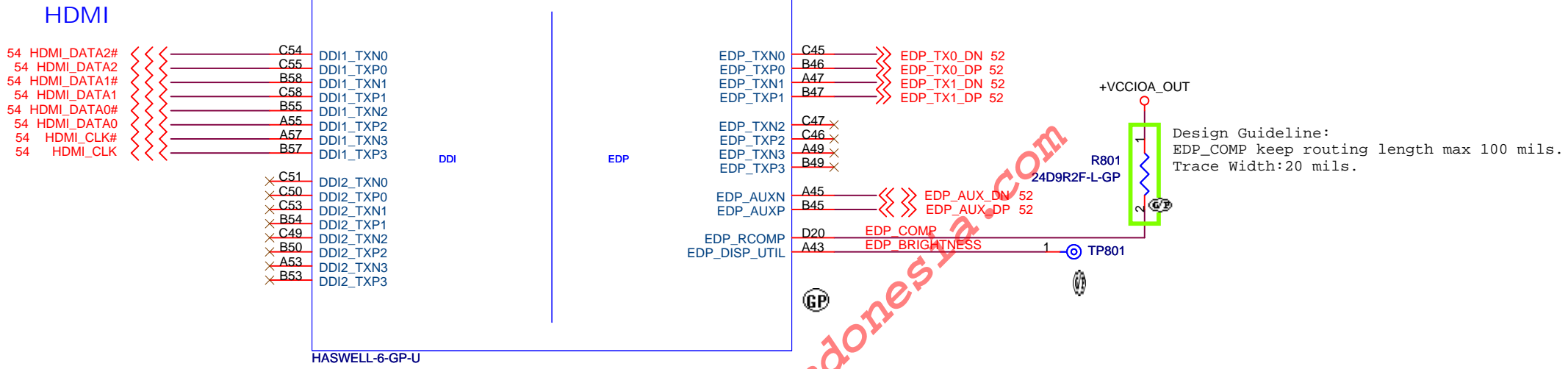


<Core Design>

DELL Wistron Corporation
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Title			CPU (VCC CORE)		
Size	Document Number	Rev			A00
A3	Hadley 17" MLK				
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SSID = CPU



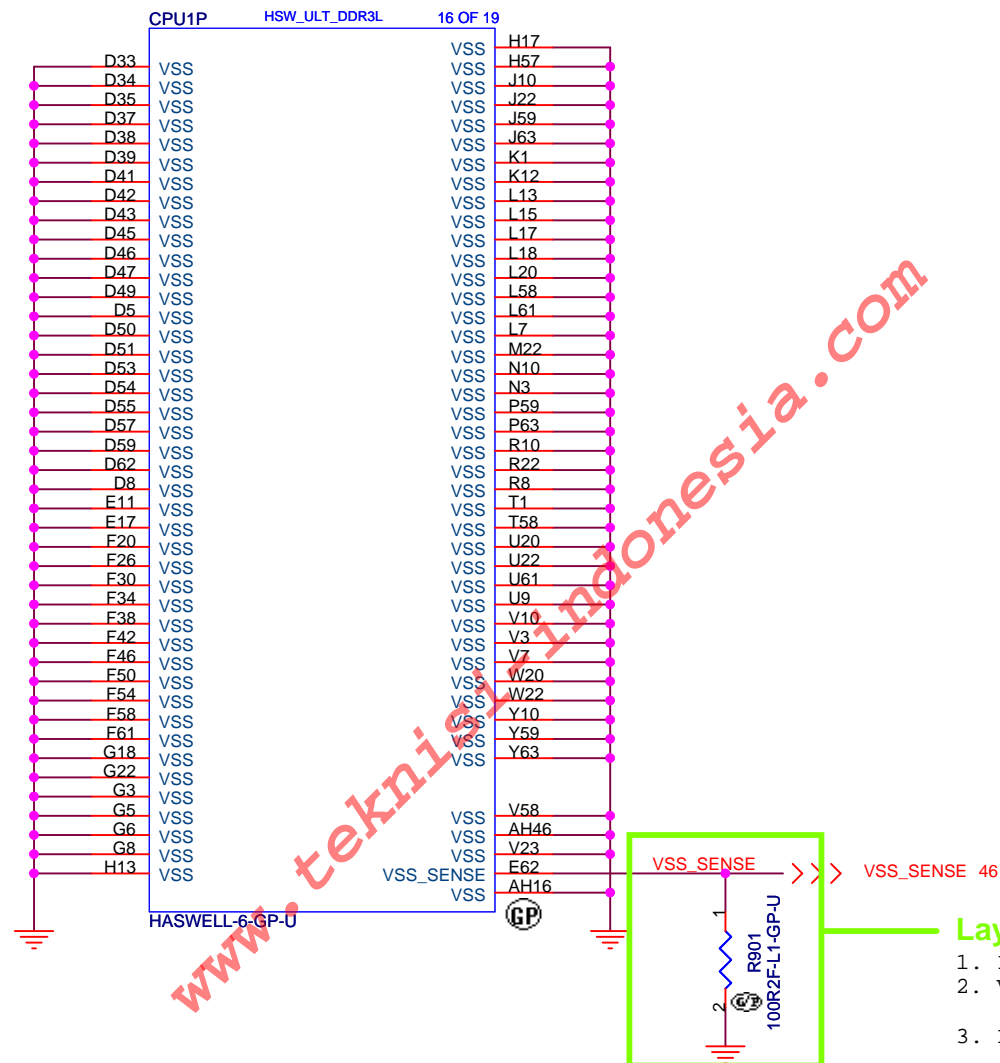
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Title			CPU (DDI/EDP)	
Size	Document Number	Rev		
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SSID = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Lwnngth match<25mil

<Core Design>



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Title

CPU (VSS)

Size
A4

Document Number

Hadley 17" MLK

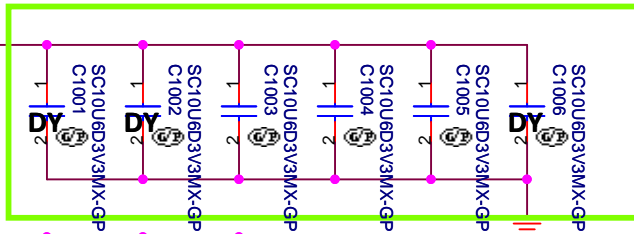
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A00

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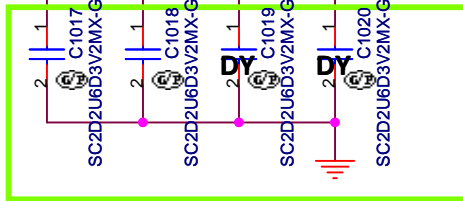
SSID = CPU

1D35V_S3



Layout Note:

As close to CPU as possible



Layout Note:

Direct tie to CPU VccIn/Vss balls

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Title

CPU(Power CAP1)

Size
A4

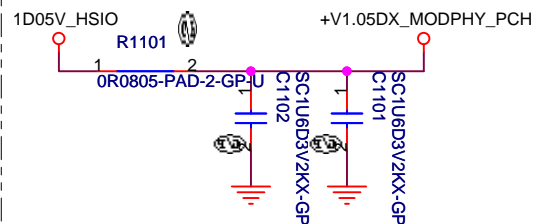
Document Number

Hadley 17" MLK

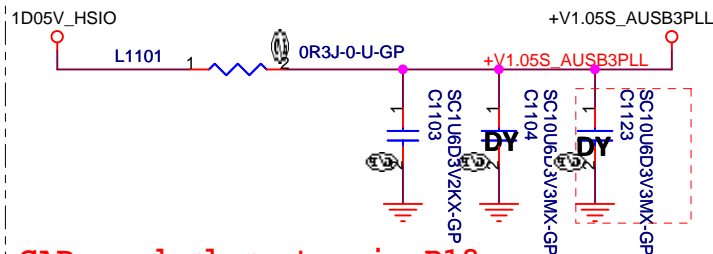
Rev
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Date: Friday, September 19, 2014

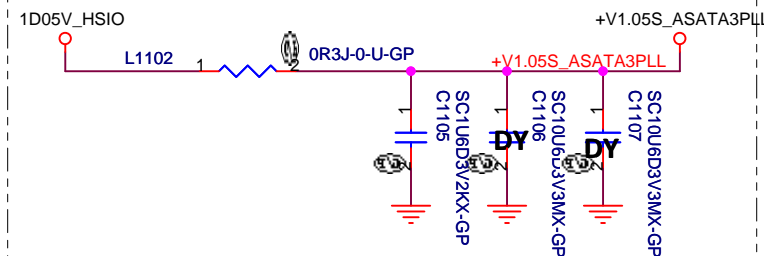
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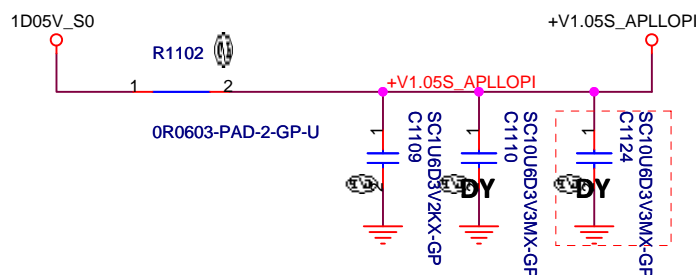
CAP need close to pin K9 L10



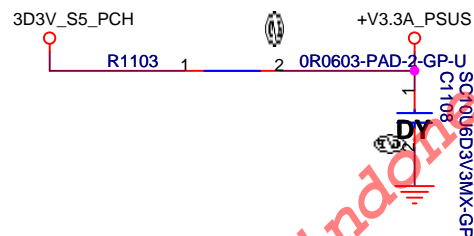
CAP need close to pin B18



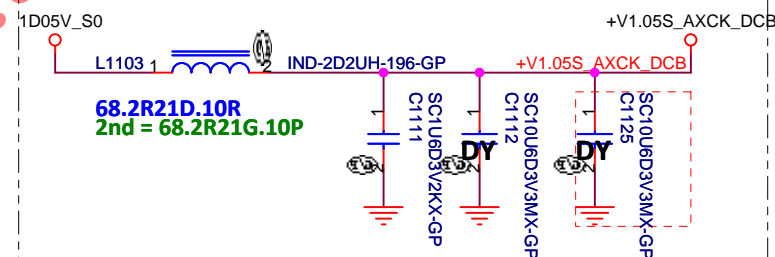
CAP need close to pin B11



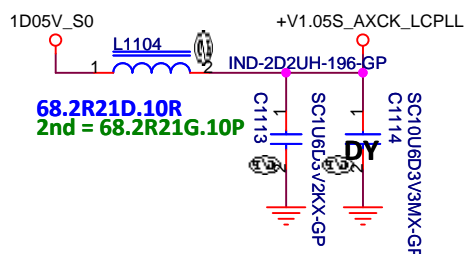
CAP need close to pin AA21



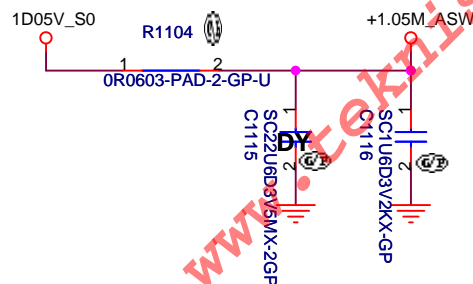
CAP need close to pin AC9



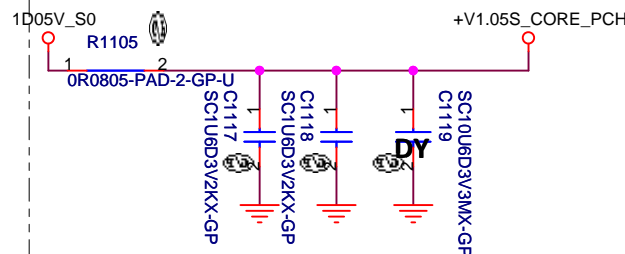
CAP need close to pin J18



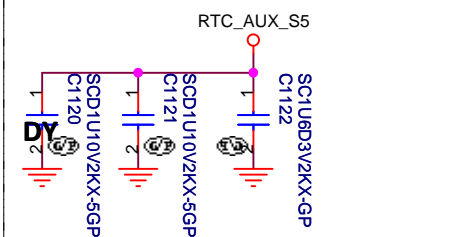
CAP need close to pin A20



CAP need close to pin AE9



CAP need close to pin AE8 J11



CAP need close to pin AG10

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Title

CPU(Power CAP2)

Size
A4

Document Number

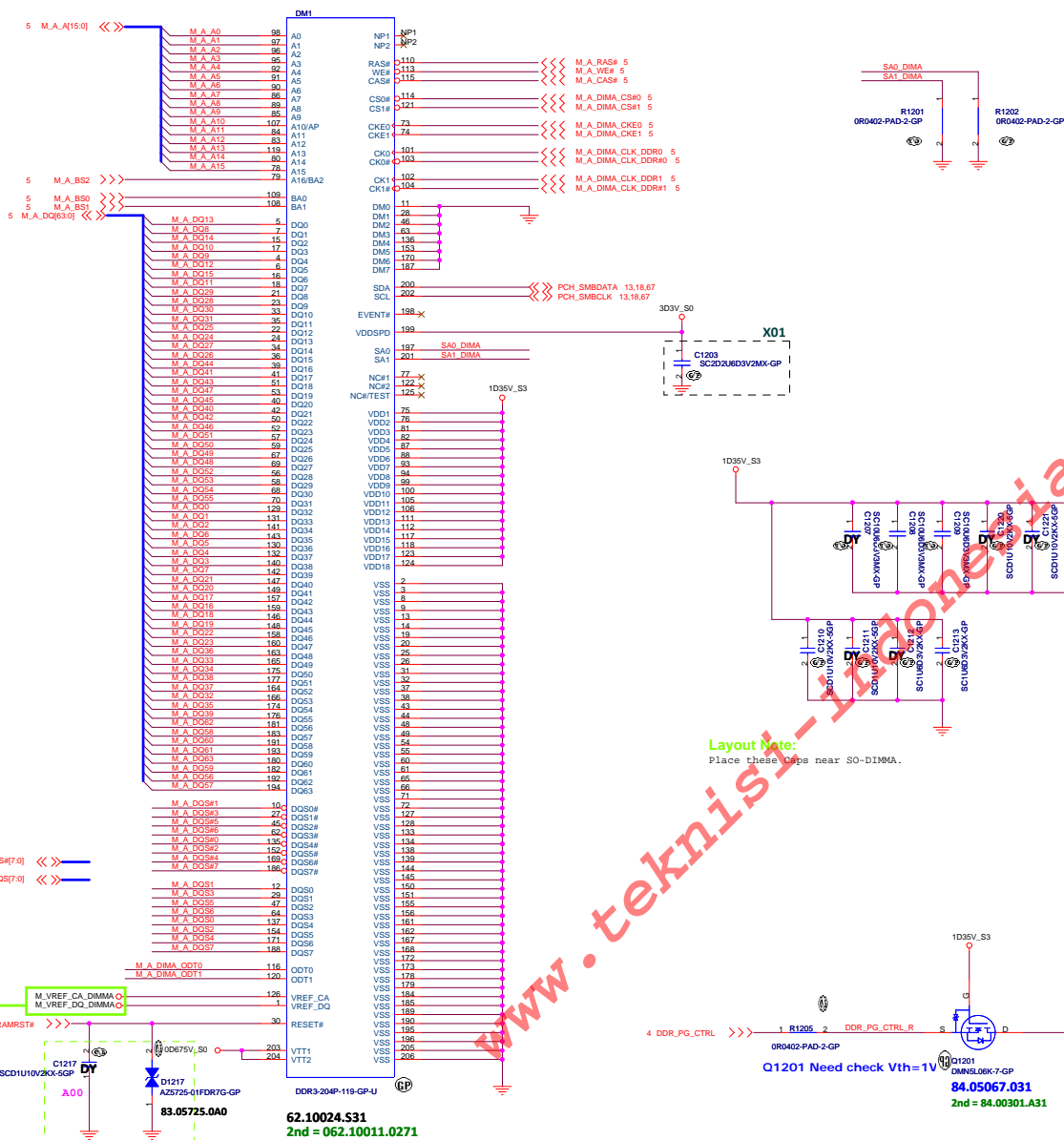
Hadley 17" MLK

Rev
A00

Date: Friday, September 19, 2014

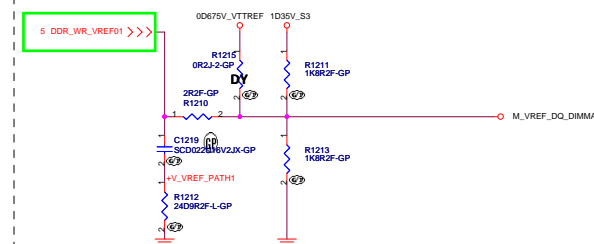
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SSID = MEMORY

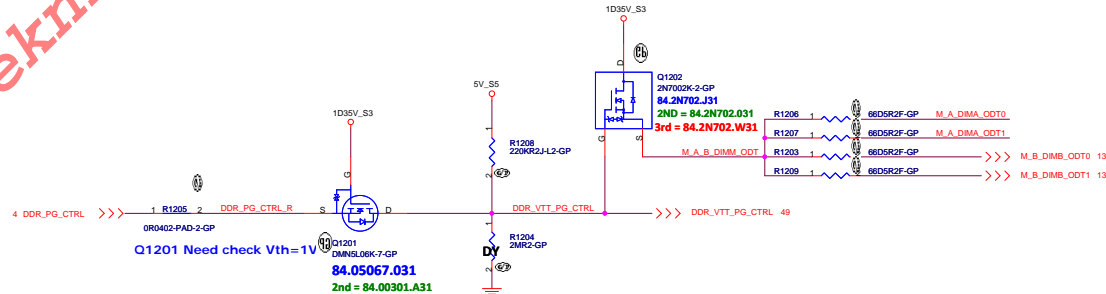


Note:
SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
CO_DIMMA TC Address is 0x20

Layout Note:
Place Close SO-DIMM.



Layout Note:
Place these Caps near SO-DIMM.



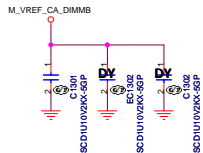
<Core Design>



SSID = MEMORY

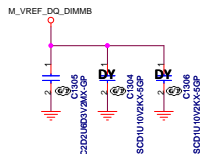
Layout Note:

Place these caps
close to VREF_CA



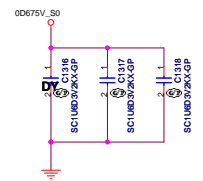
Layout Note:

Place these caps
close to VREF_DQ



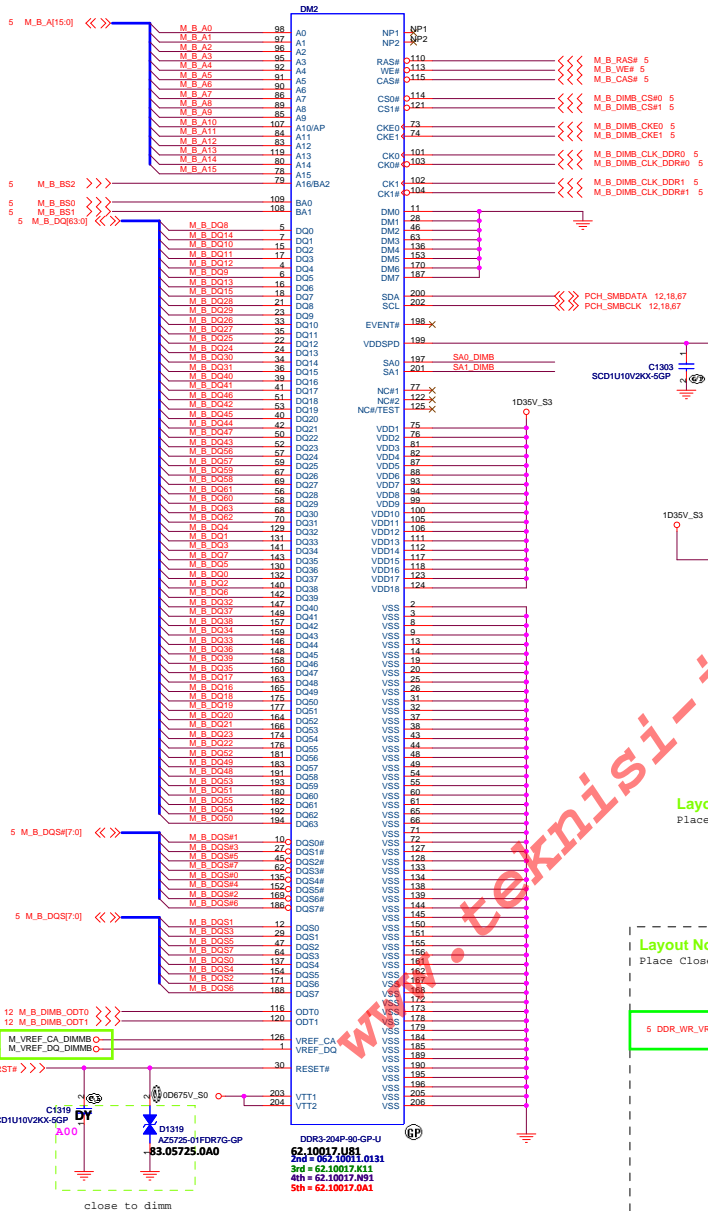
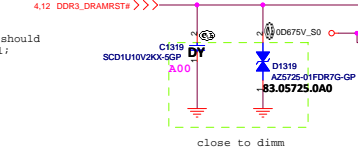
Layout Note:

Place these caps
close to VTT1 and
VTT2.



Layout Note:

All VREF traces should
have width=20mil;
spacing=20 mil

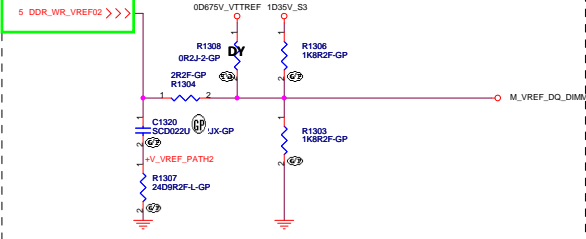


Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

Layout Note:
Place these Caps near SO-DIMMA.

Layout Note:

Place Close SO-DIMMA.



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Title

M1&M3

Size
A3

Document Number

Hadley 17" MLK

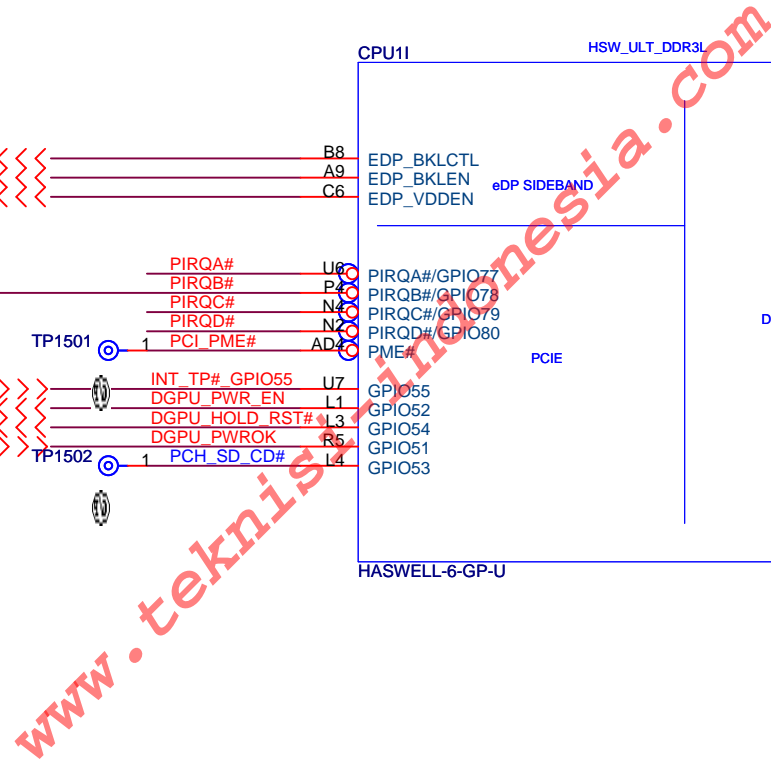
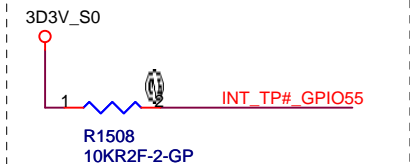
Rev

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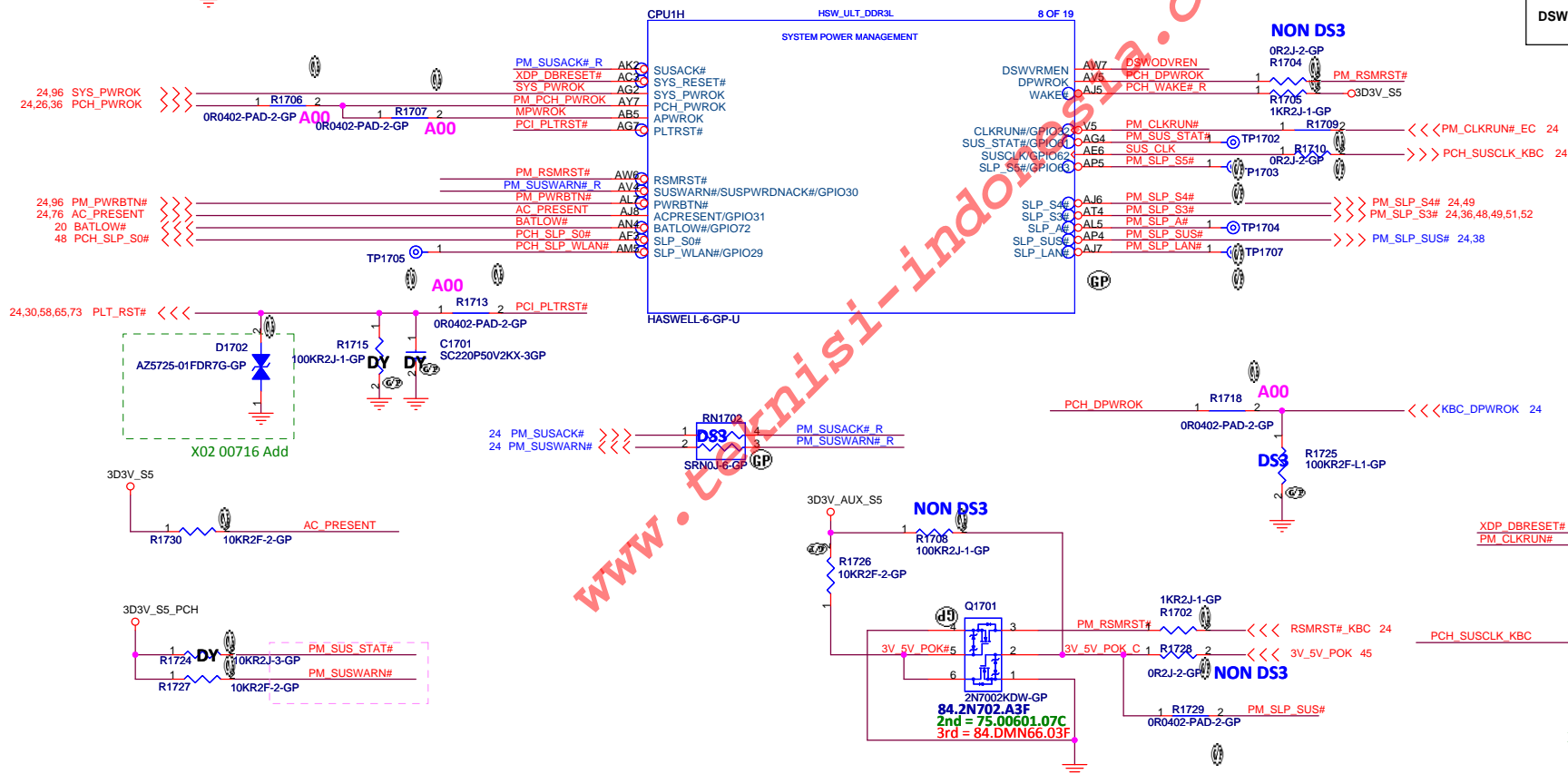
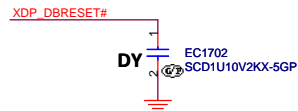
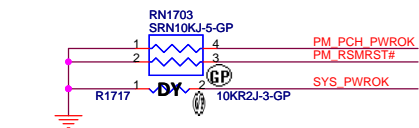
SSID = CPU



Title	CPU (EDP SIDEBAND/GPIO/DDI)
-------	--------------------------------------

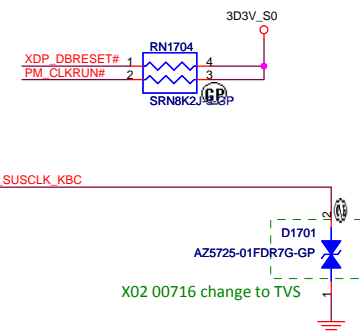
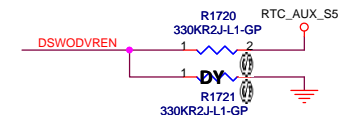
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SSID = CPU



PCH strap pin:

On Die DSW VR Enable	
DSWODVREN	Low = Disable ★ High = Enable (default)



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Title

CPU (PM)

Size
A3

Document Number

Hadley 17" MLK

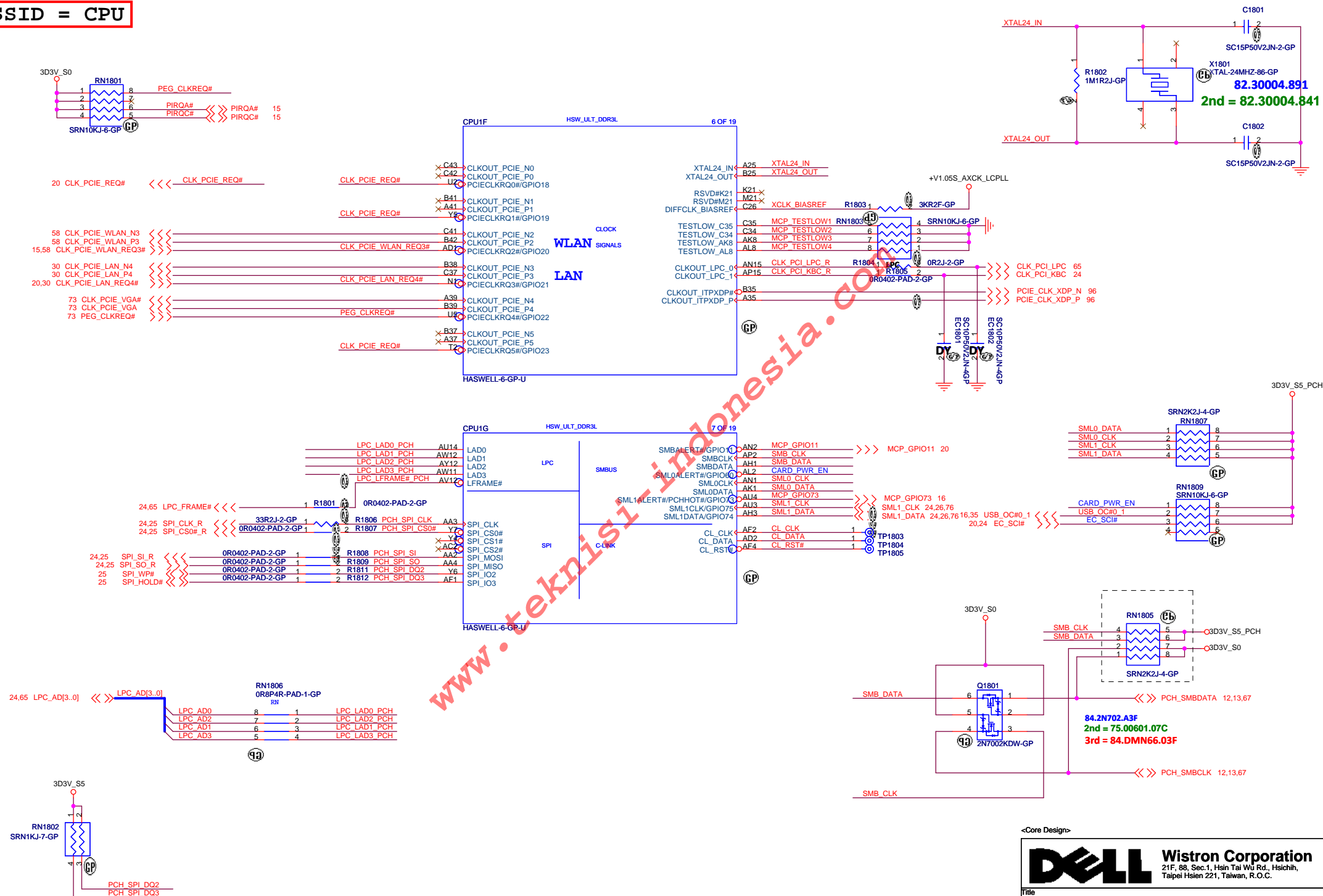
Rev
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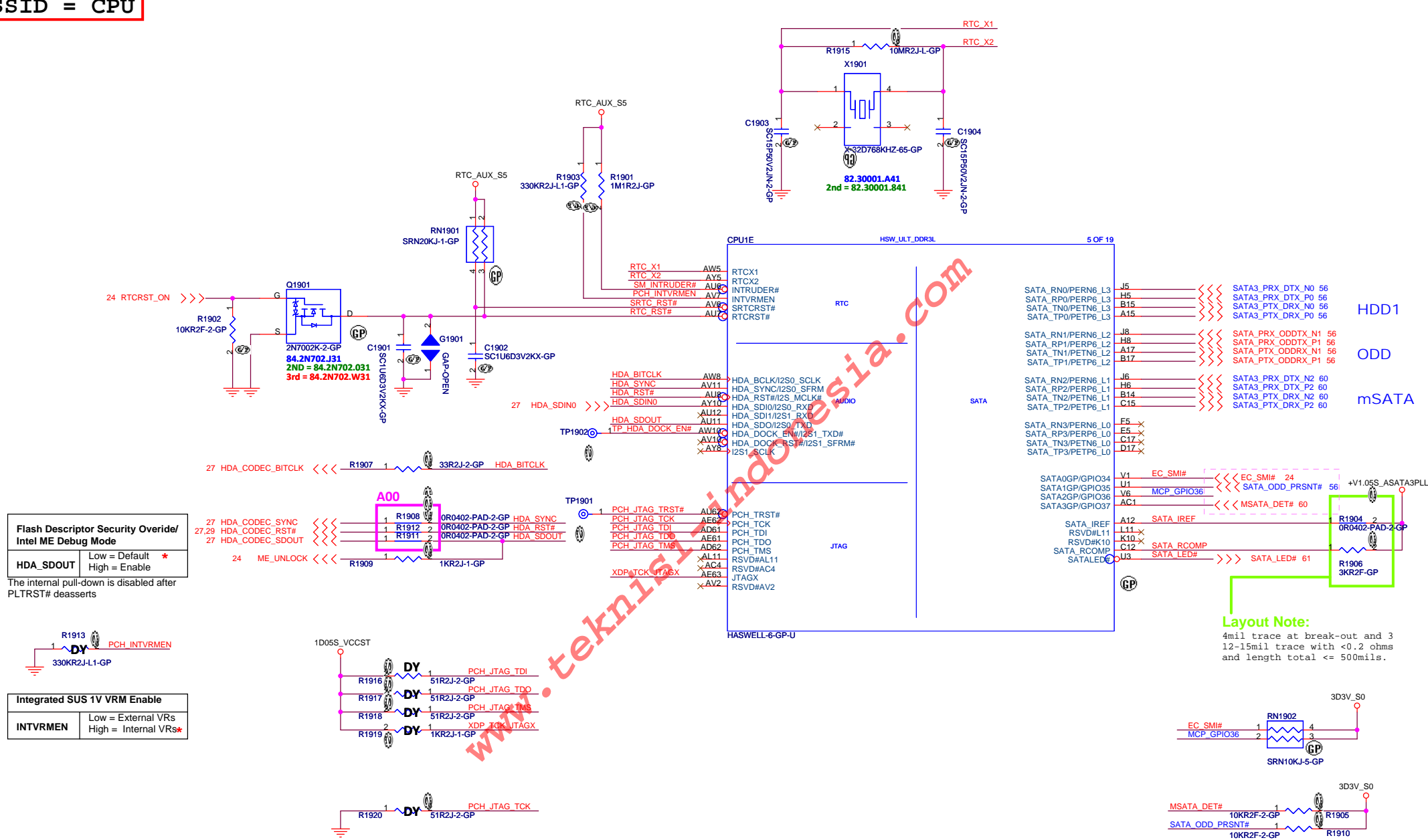
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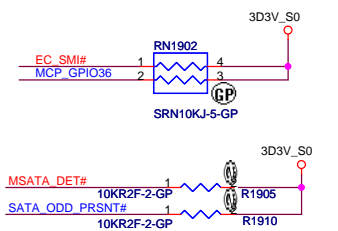
SSID = CPU



SSID = CPU



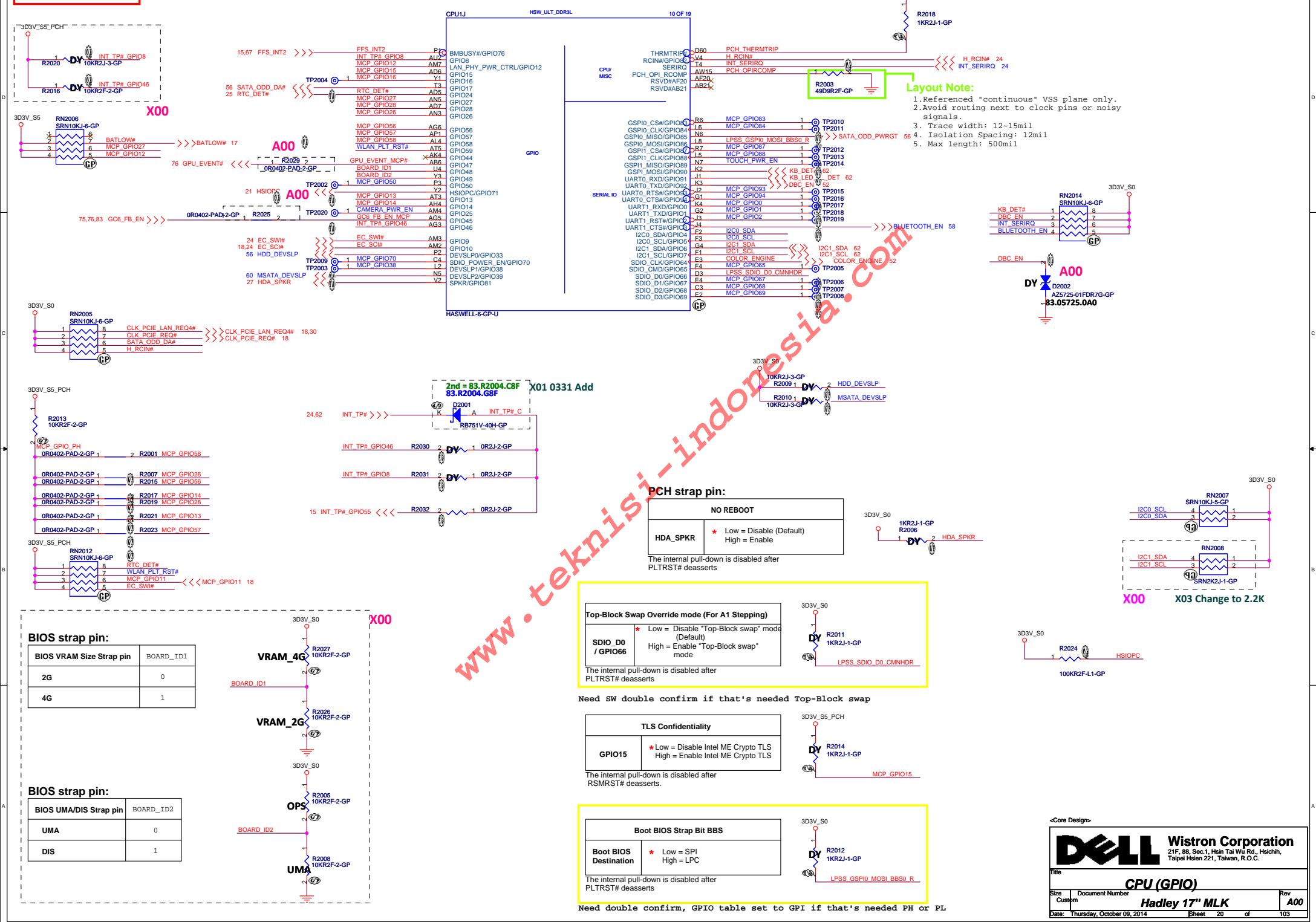
Layout Note:
4mil trace at break-out and 3
12-15mil trace with <0.2 ohms
and length total ≤ 500 mils.



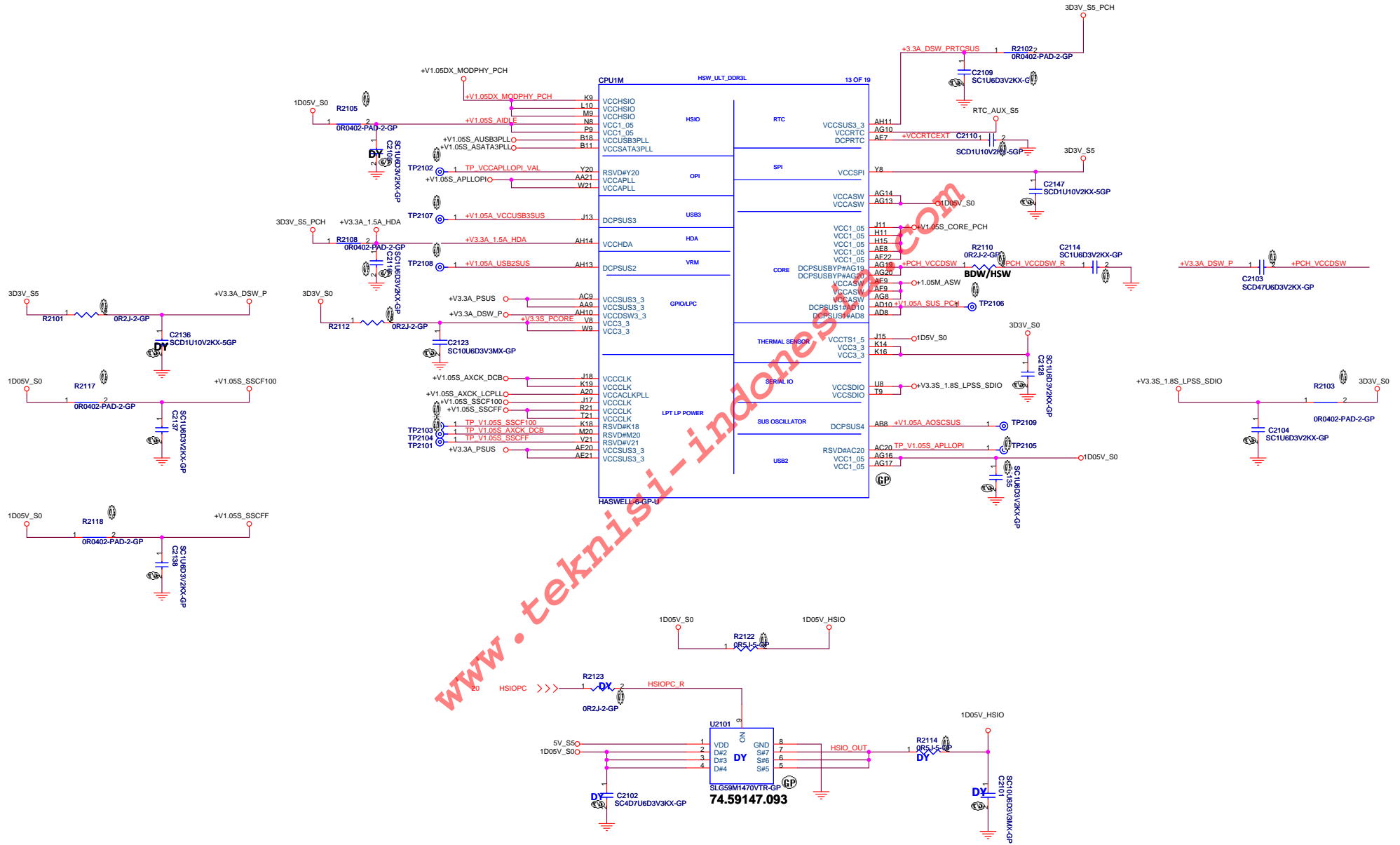
Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default ★ High = Enable

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

SSID = CPU



SSID = CPU



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Title

CPU (POWER2)

Size	D
Custom	

Document Number

Hadley 17" MLK

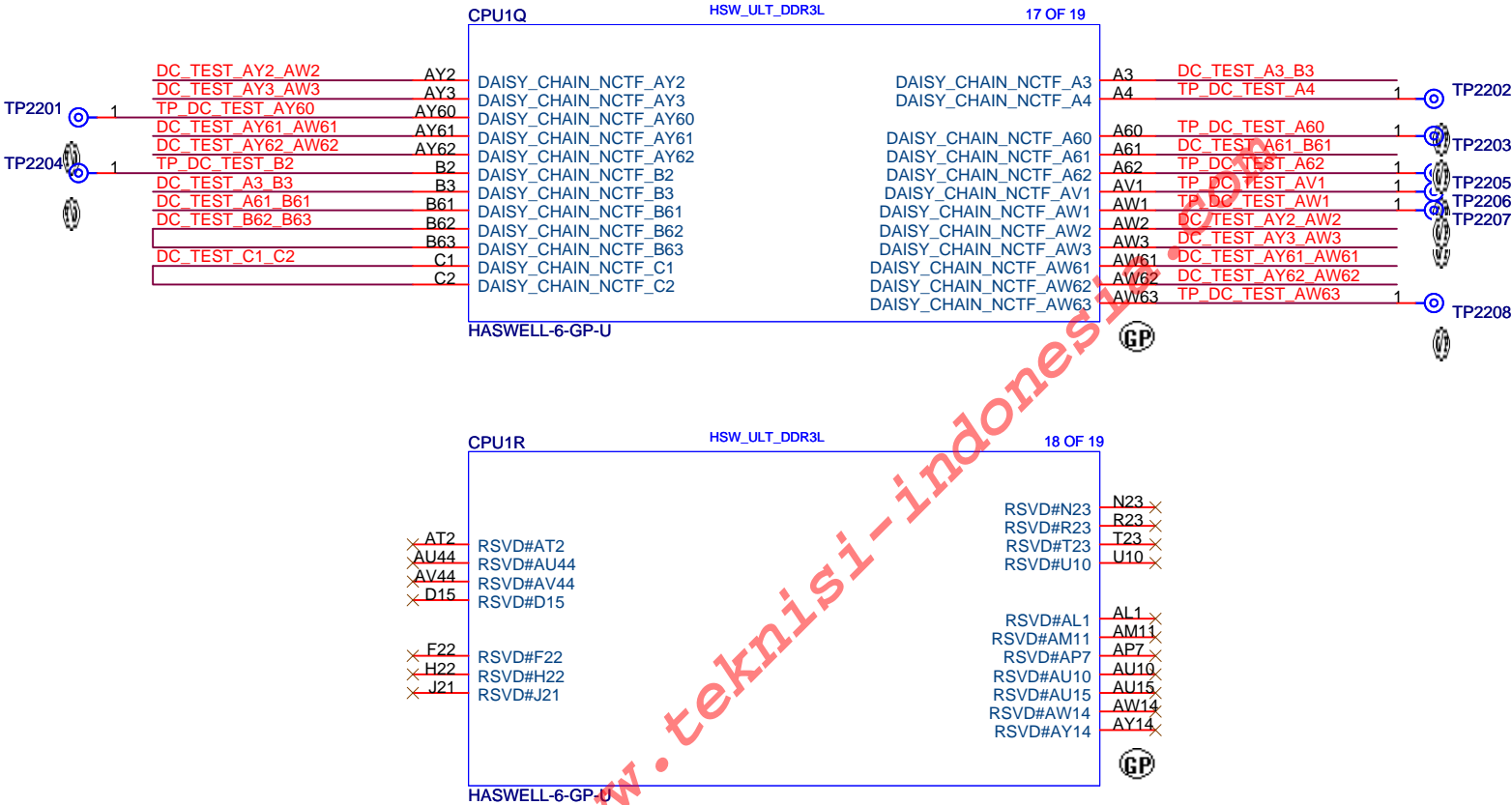
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SSID = CPU



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Title

RSVD

Size

A4

Document Number

Hadley 17" MLK

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A00

Date

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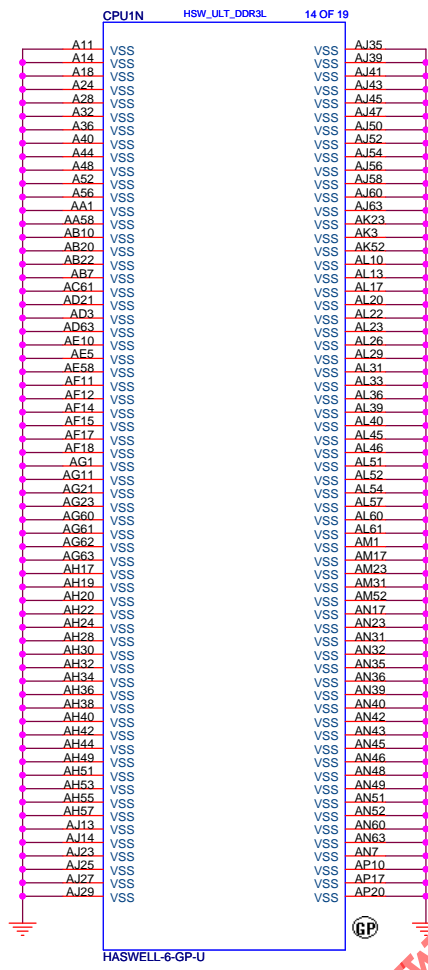
Sheet

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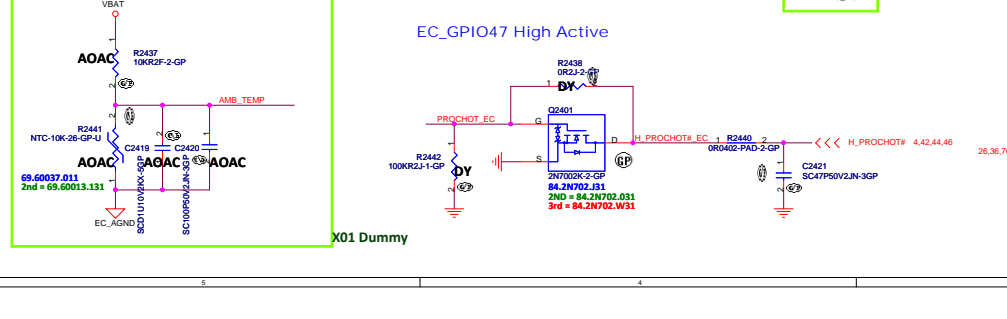
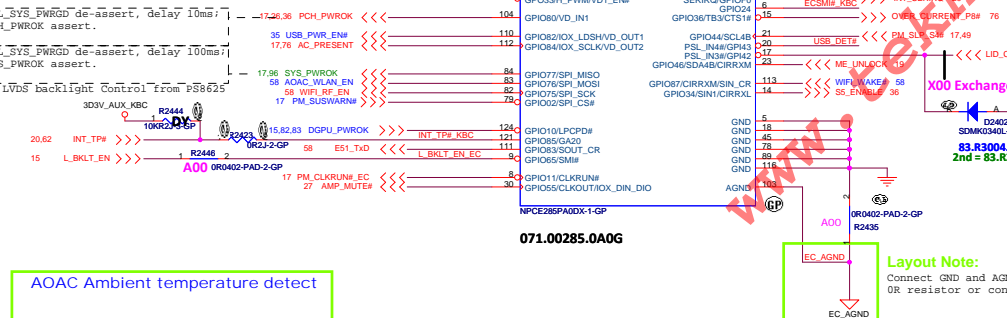
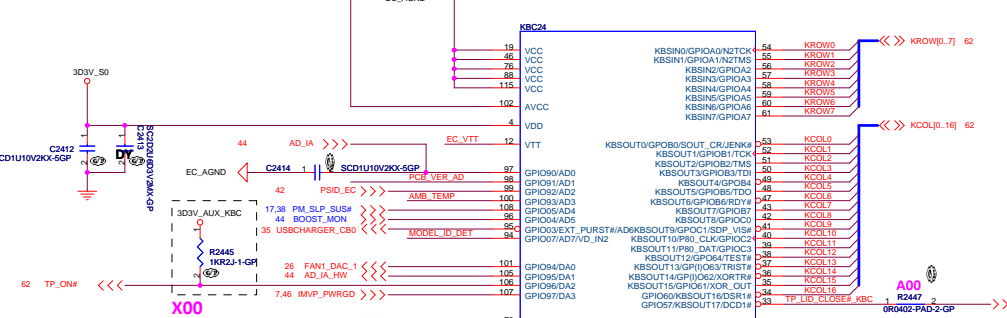
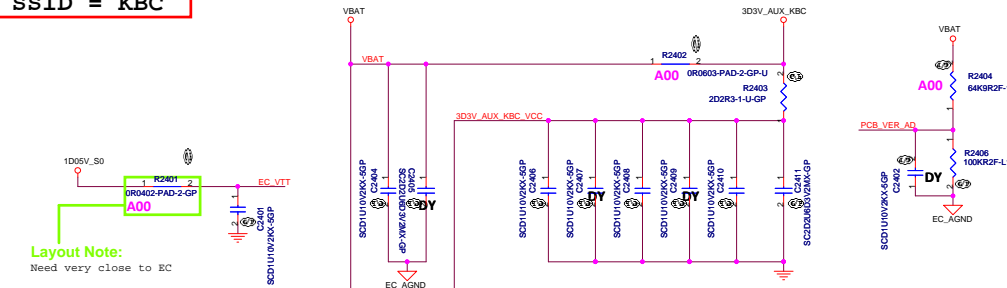
of

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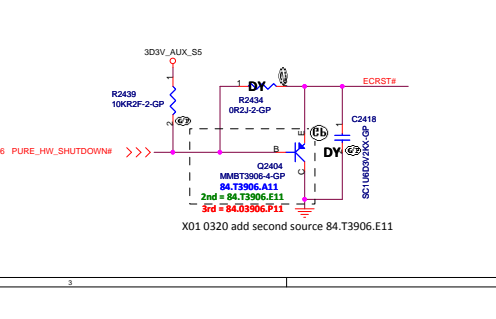
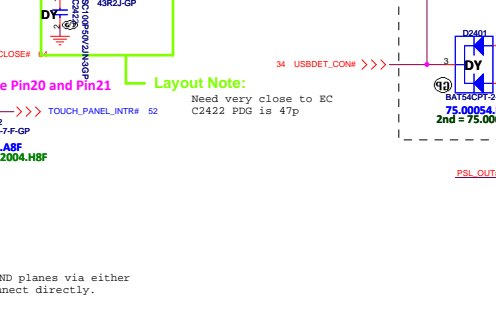
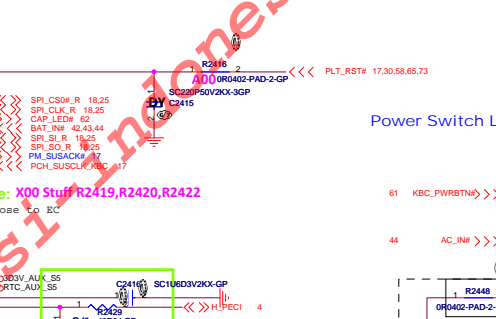
SSID = CPU



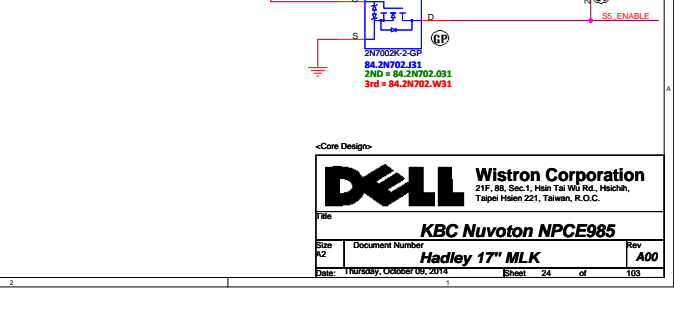
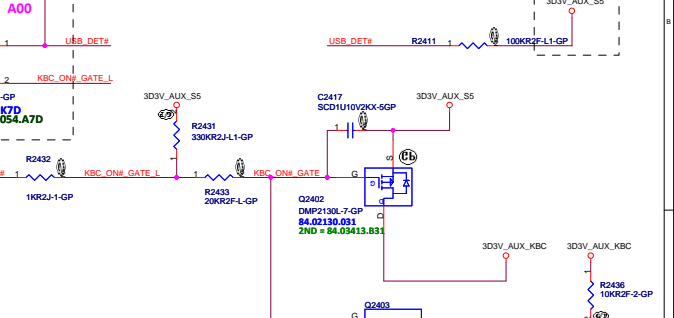
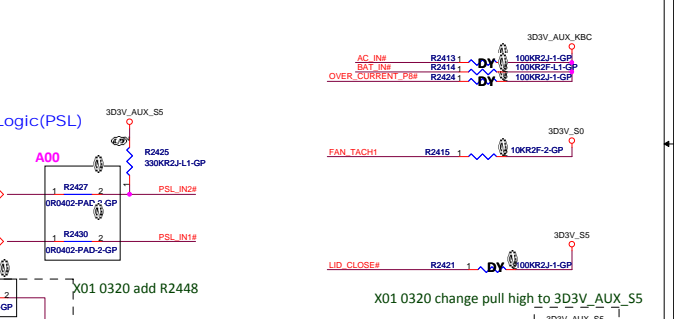
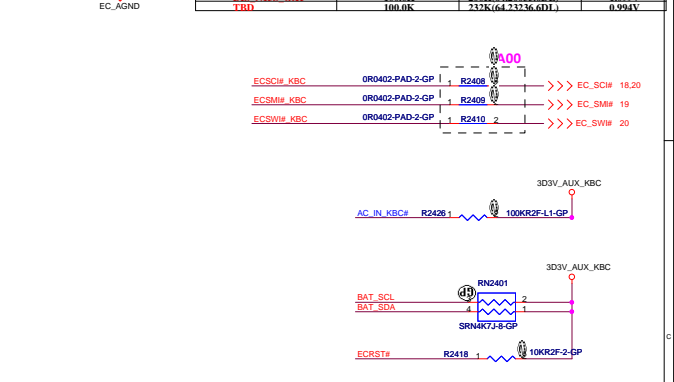
SSID = KBC



PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

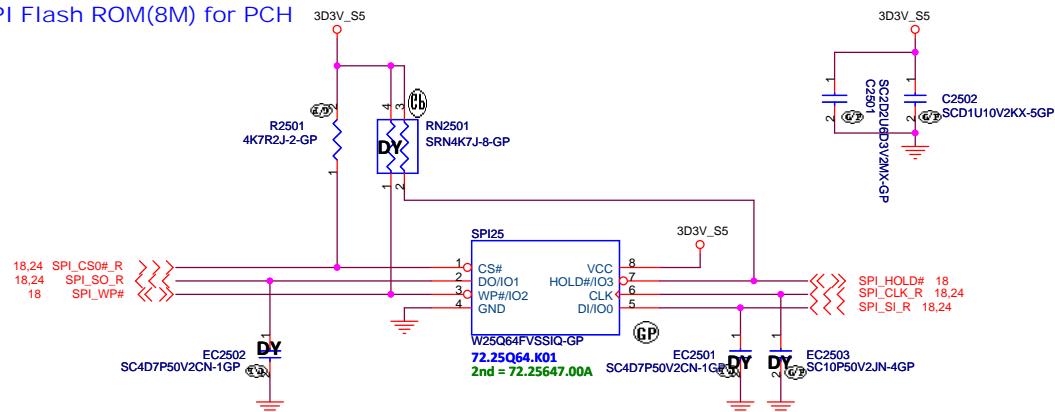


MODEL_ID_DET(GPI07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1A0	100.0K	10.0K	3.0V
1B0	100.0K	13.7K	2.902V
1C0	100.0K	17.8K	2.801V
1D0	100.0K	22.1K	2.702V
1E0	100.0K	27.0K	2.593V
1F0	100.0K	32.4K	2.493V
1G0	100.0K	37.4K	2.402V
1H0	100.0K	43.2K	2.304V
1I0	100.0K	49.9K	2.204V
1J0	100.0K	57.6K	2.093V
1K0	100.0K	64.9K	2.000V
1L0	100.0K	73.2K	1.902V
1M0	100.0K	82.5K	1.808V
1N0	100.0K	93.1K	1.709V
1O0	100.0K	107K	1.594V
1P0	100.0K	130K	1.493V
1Q0	100.0K	137K	1.392V
1R0	100.0K	154K	1.290V
1S0	100.0K	200K	1.093V
1T0	100.0K	232K	0.994V



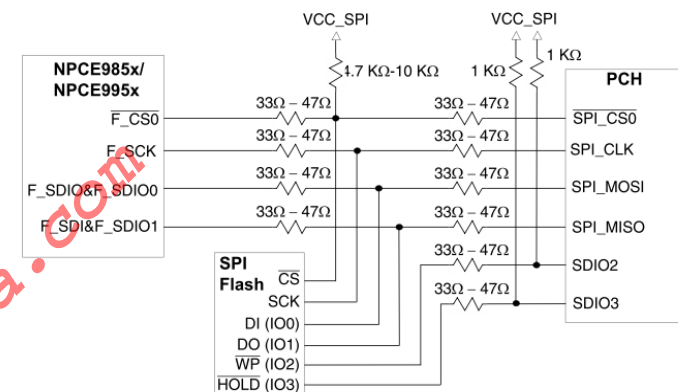
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



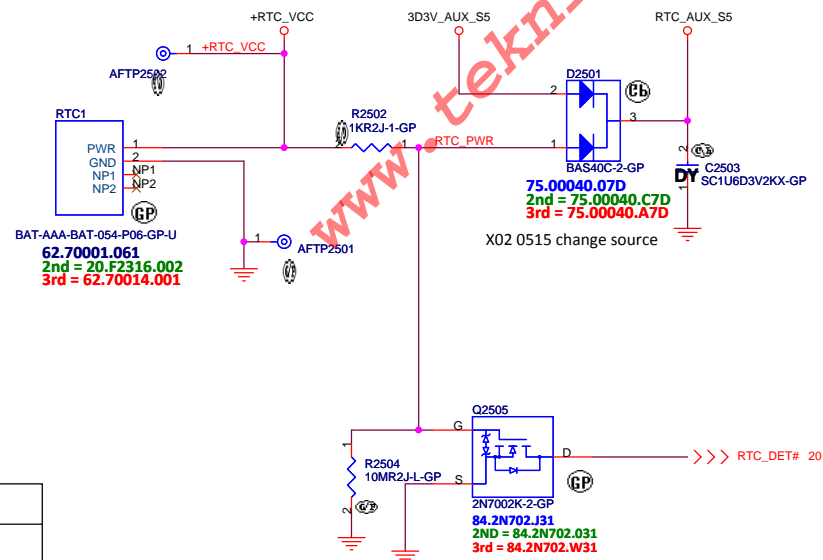
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	0	0
72.25647.00A	0	0

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NPCE985x/ NPCE995x board design reference guide"

SSID = RBATT



2032 Battery

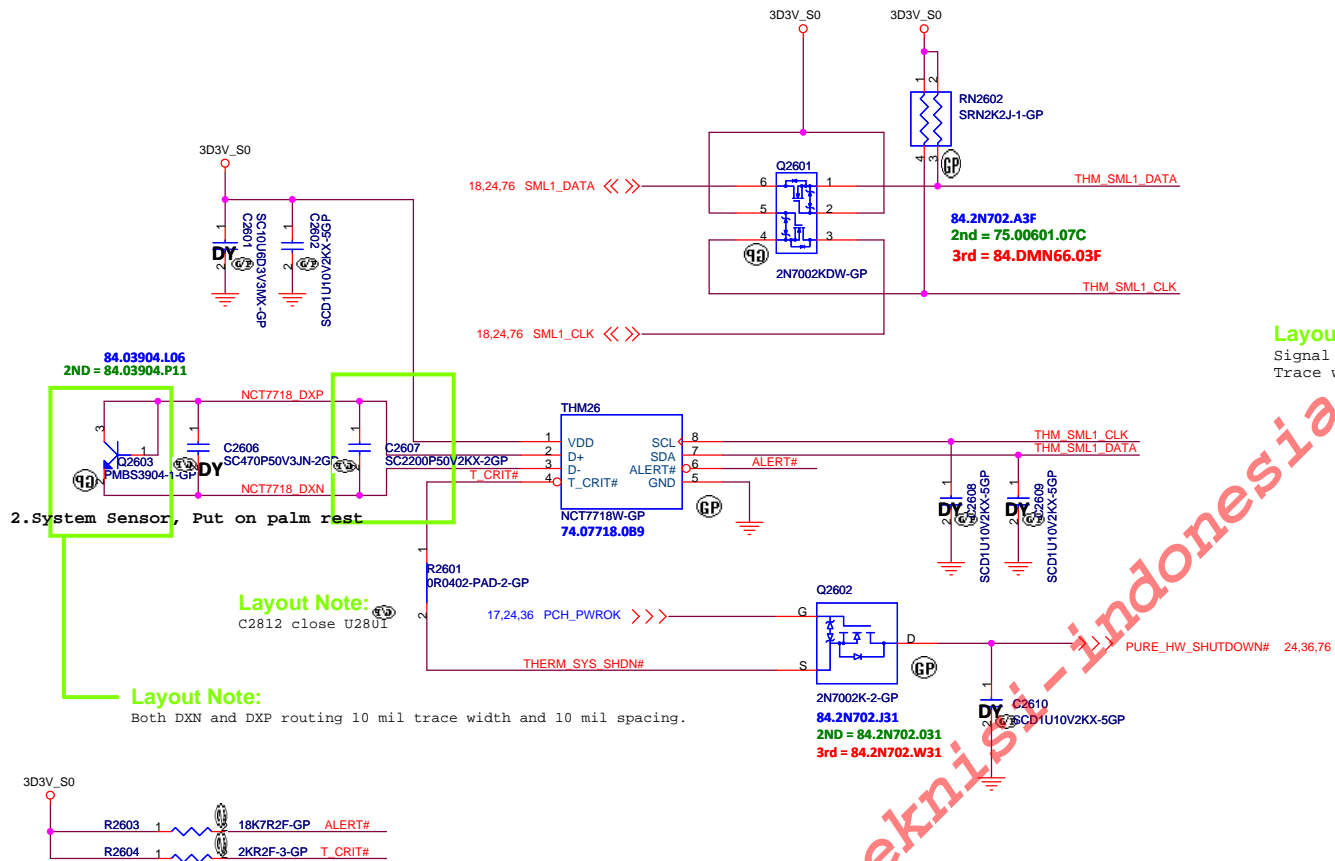
隆電	23.22063.001
仕野	23.22068.001

<Core Design>

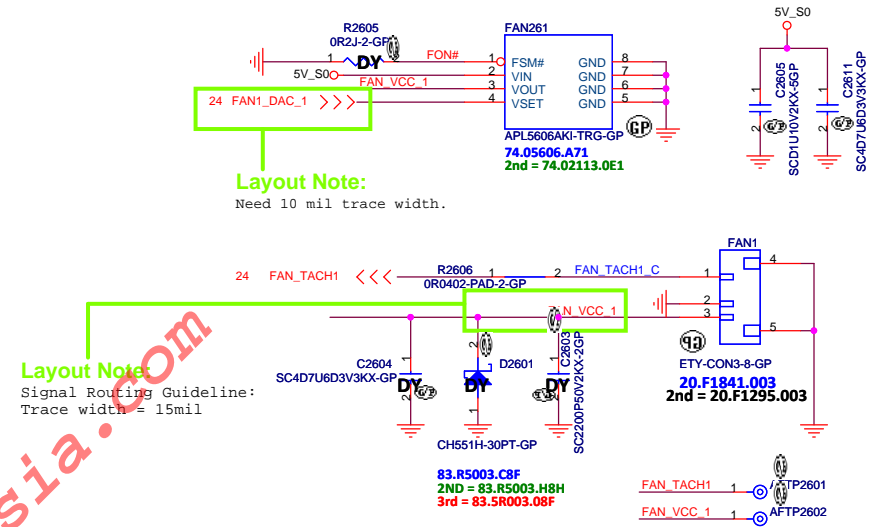
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Title	Flash/RTC	
Size	Document Number	Rev
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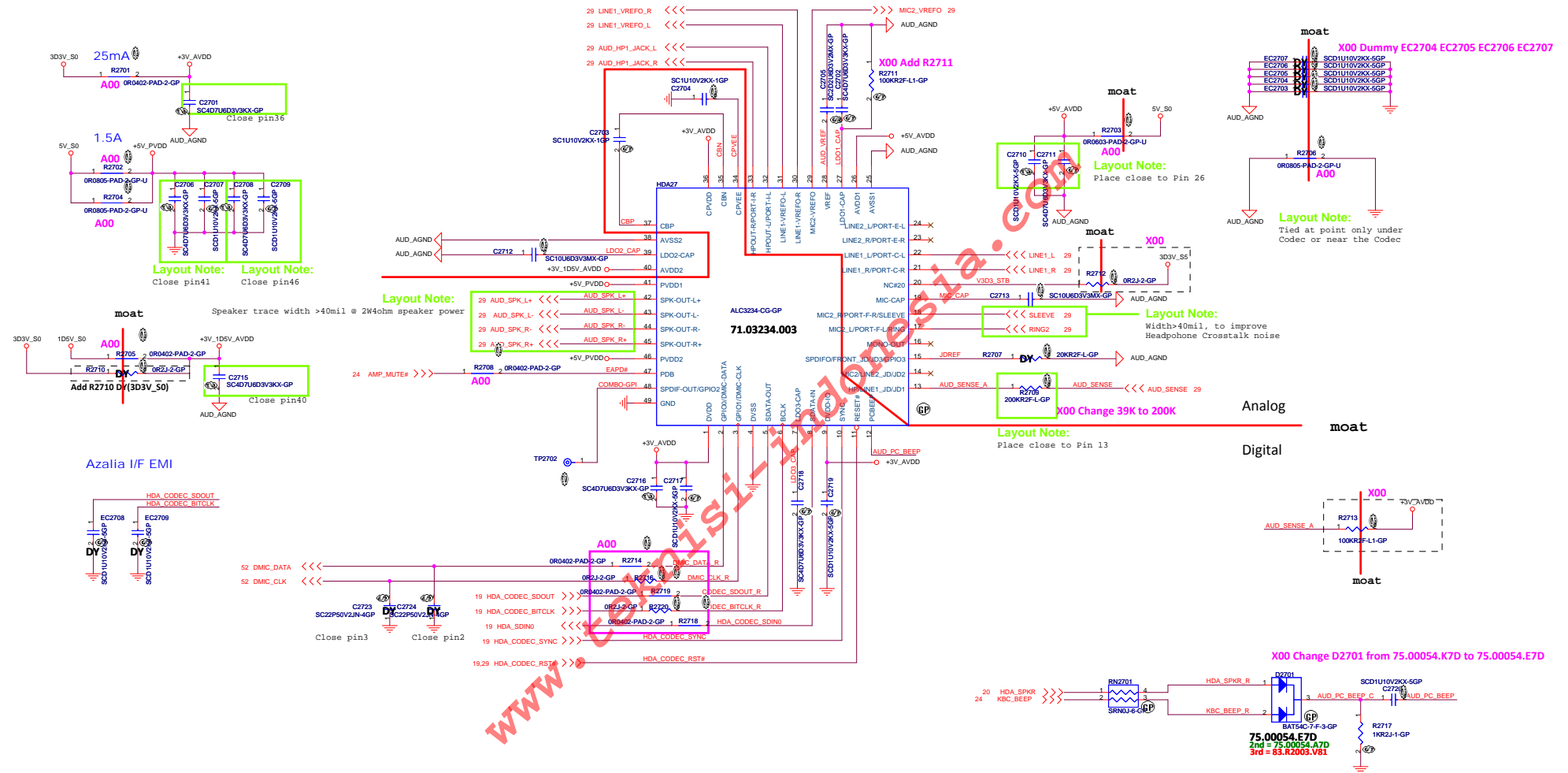
SSID = Thermal



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



SSID = AUDIO



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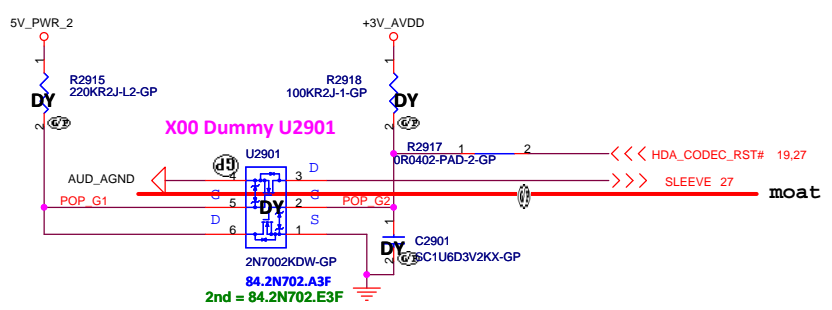
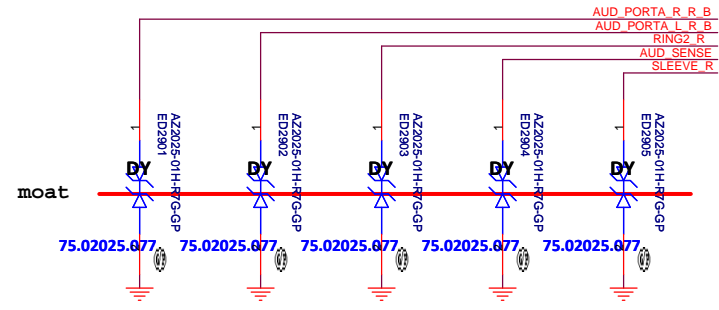
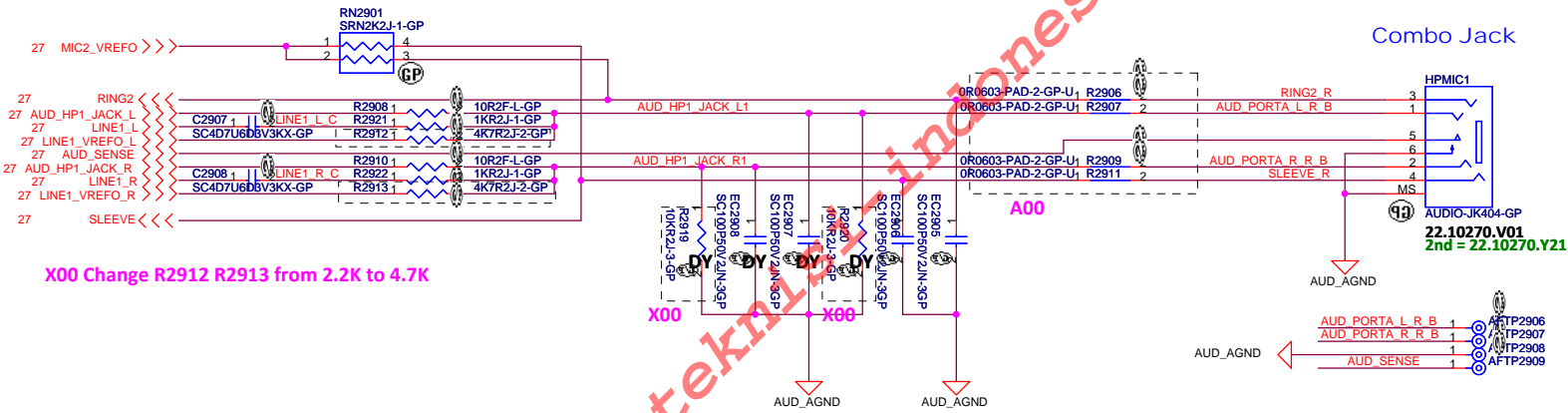
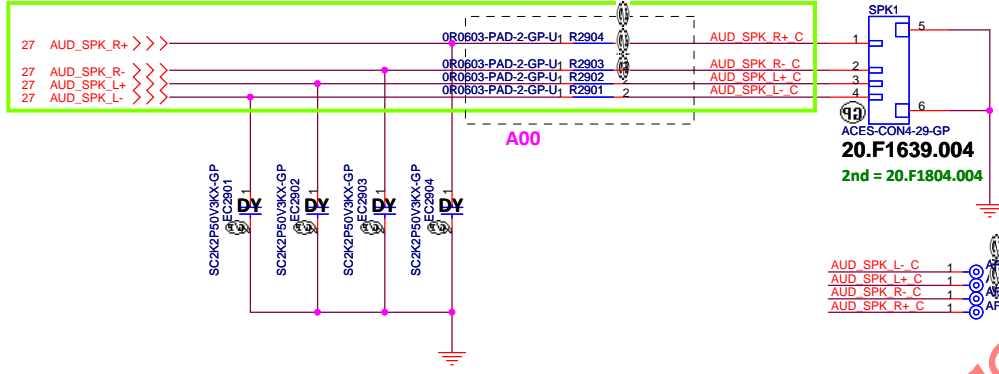
Title

Reserved

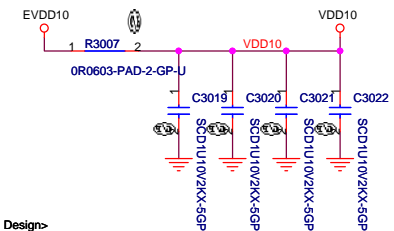
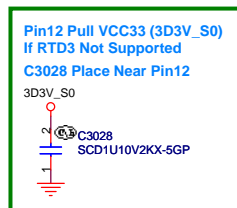
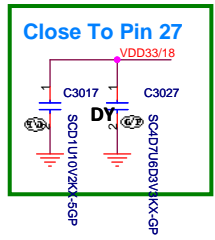
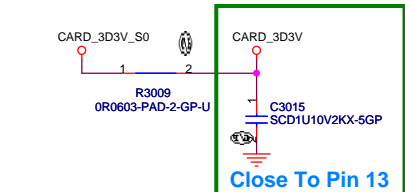
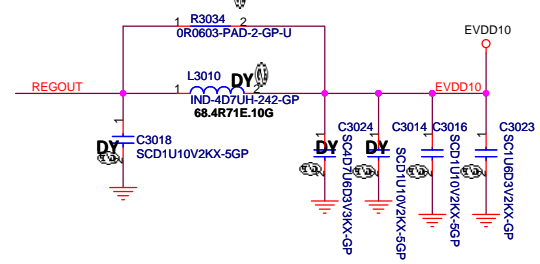
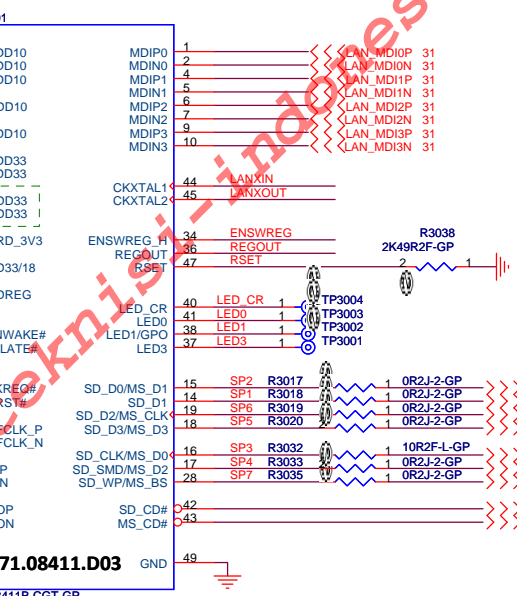
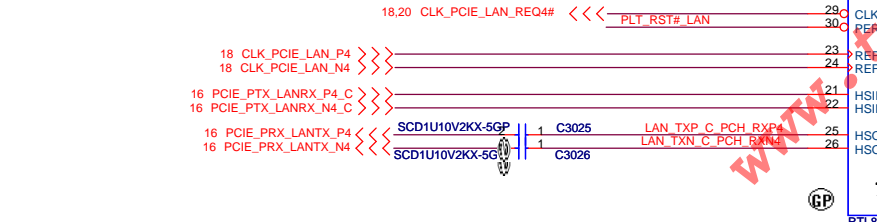
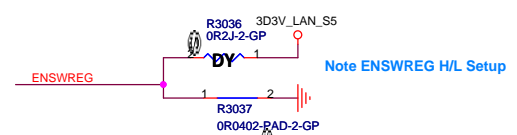
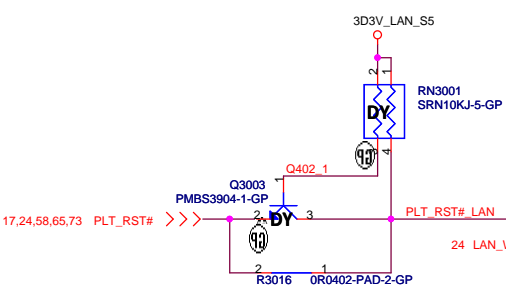
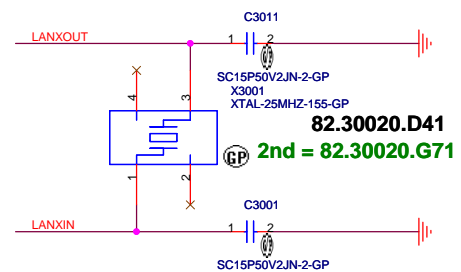
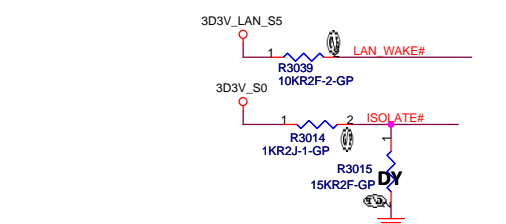
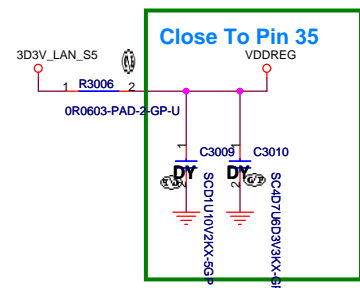
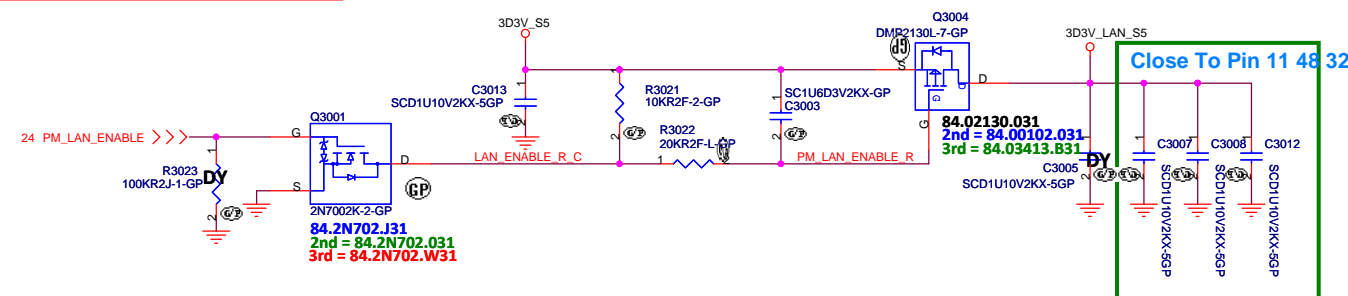
Size	Document Number	Rev
A3	Hadley 17" MLK	A00

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----------------------------------	-----------------

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

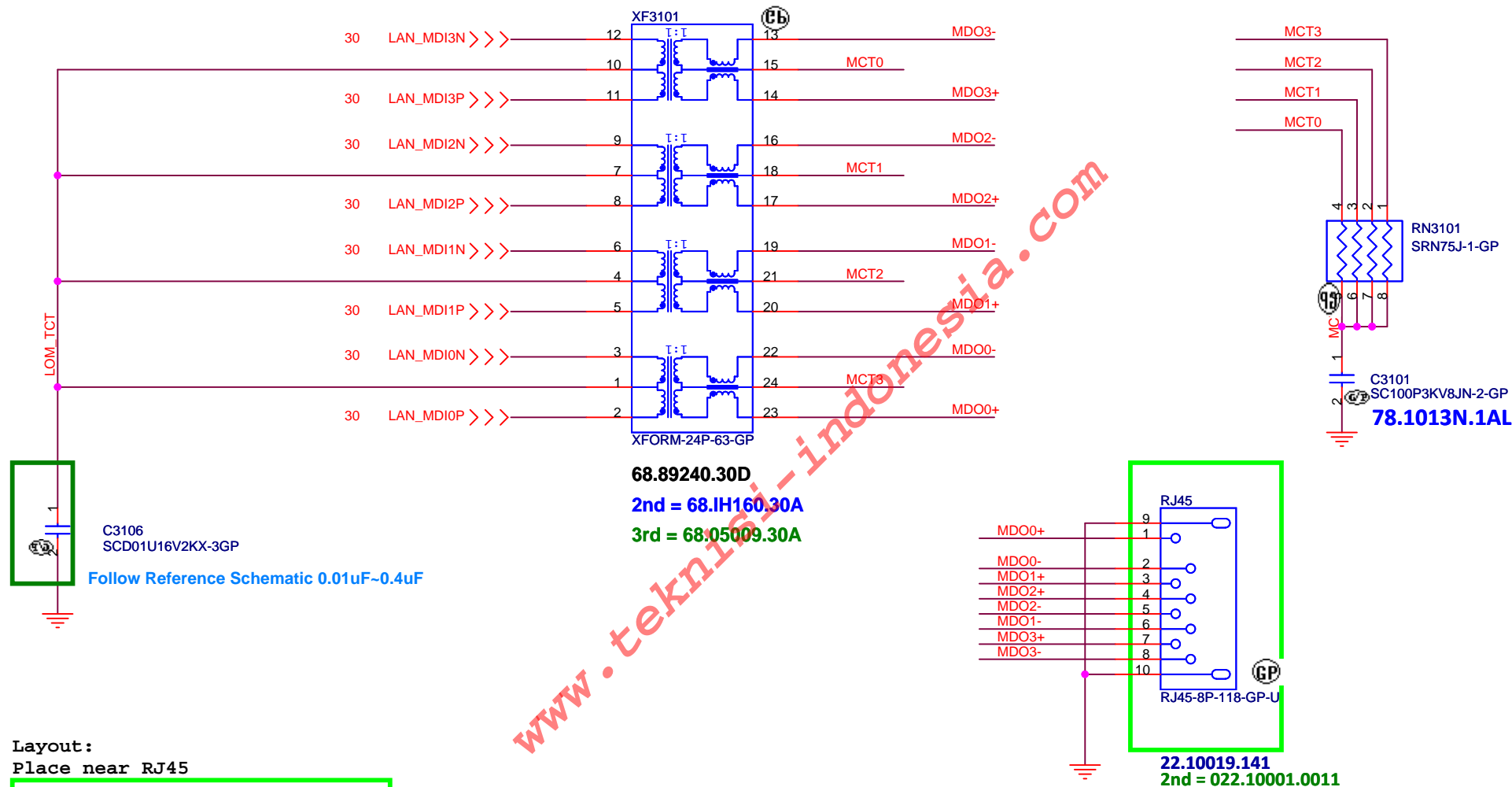


SSID = LAN CHIP

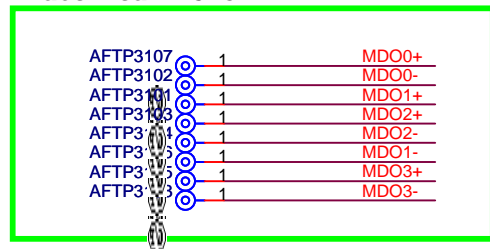


SSID = LOM

GIGA LAN TransFormer



Layout:
Place near RJ45



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Title

RJ45+Transformer

Size	A4
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Title

Card Reader(RTS5176)

Size
A3

Document Number

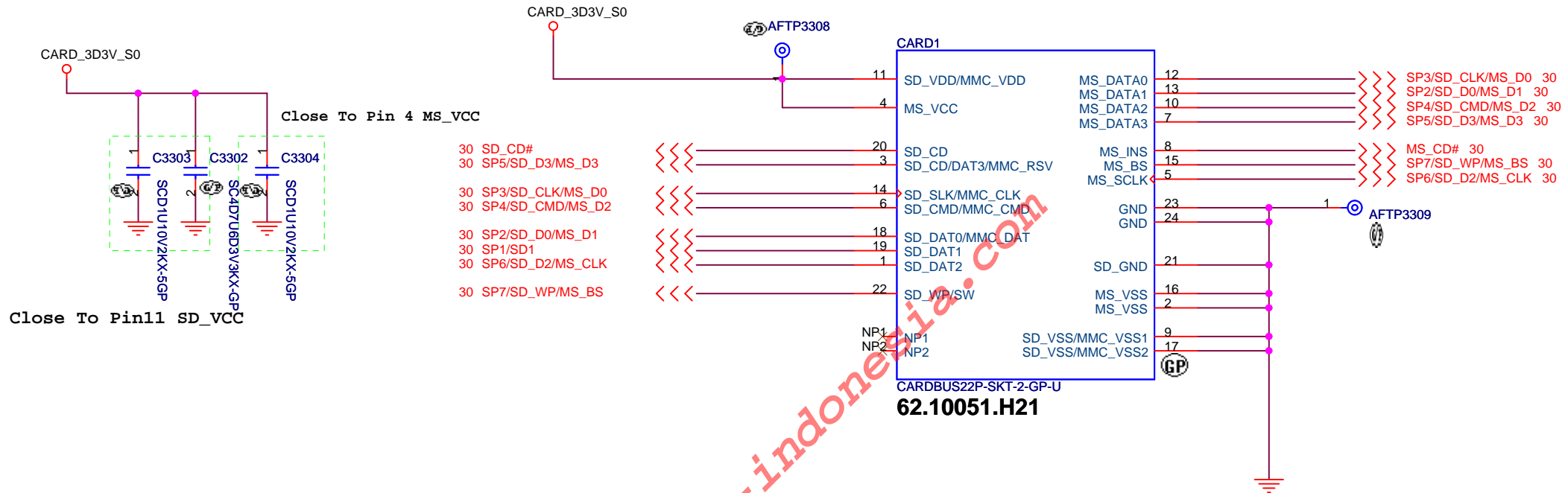
Hadley 17" MLK

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A00

Date: Friday, September 19, 2014

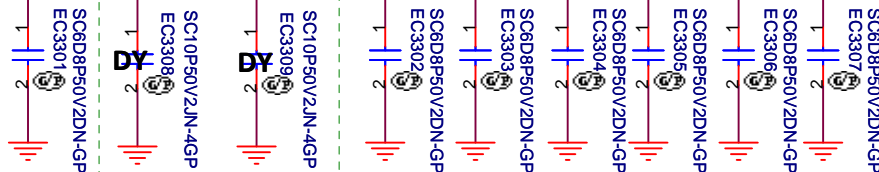
Sheet 32 of 103

SSID = SDIO

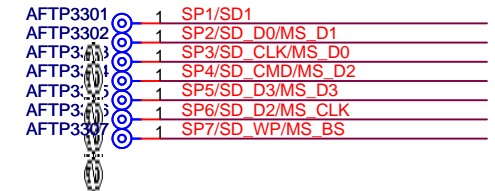


Reserve EMI Cap, CLK Pop

SP1/SD1
SP2/SD_D0/MS_D1
SP3/SD_CLK/MS_D0
SP4/SD_CMD/MS_D2
SP5/SD_D3/MS_D3
SP6/SD_D2/MS_CLK
SP7/SD_WP/MS_BS



X02 00716 Add



<Core Design>

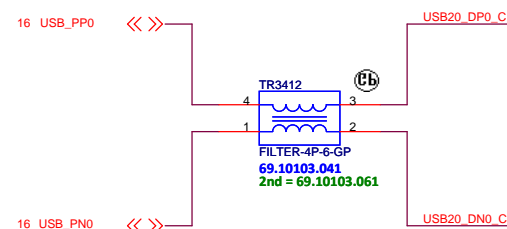
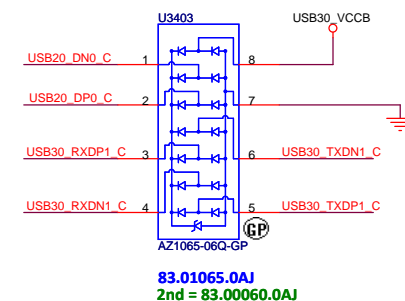
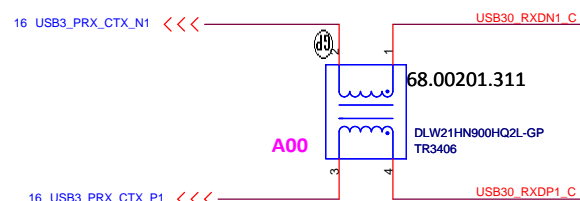
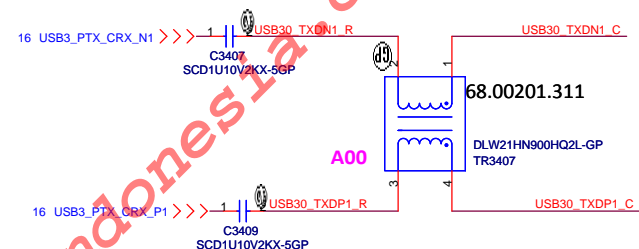
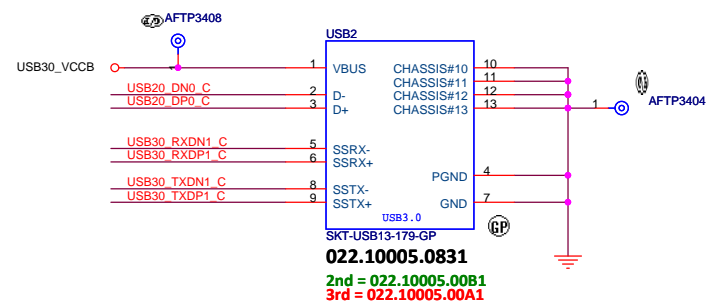
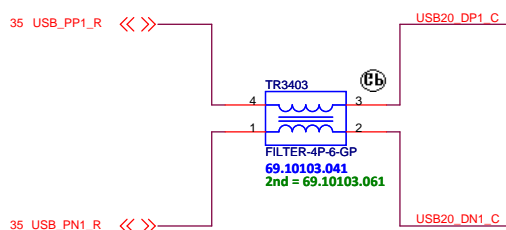
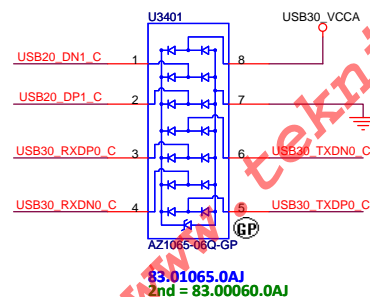
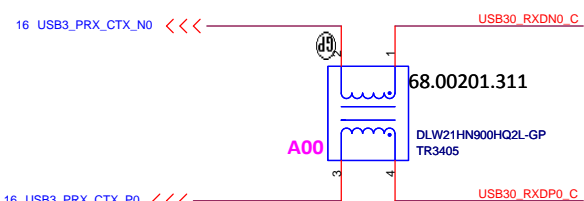
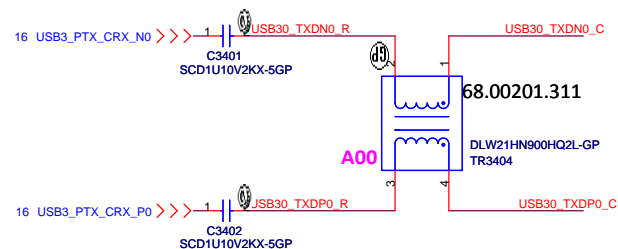
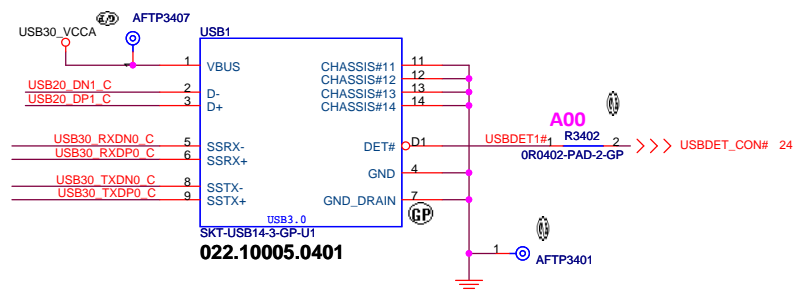


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Title Card Reader CONN		
Size A4	Document Number Hadley 17" MLK	Rev A00
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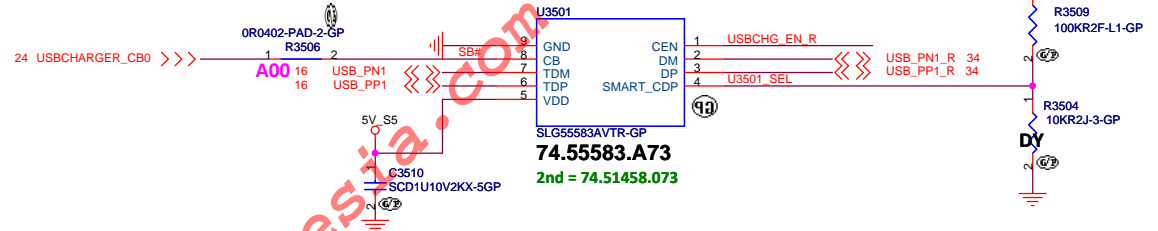
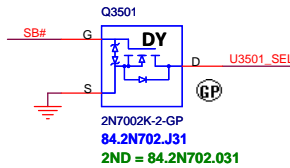
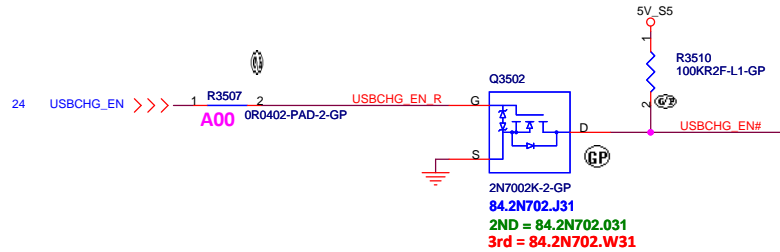
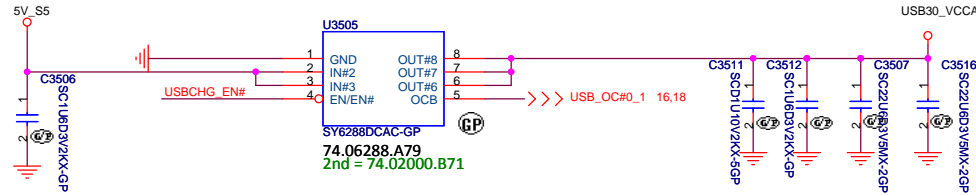
SSID = USB

USB3.0 Port1 with power share



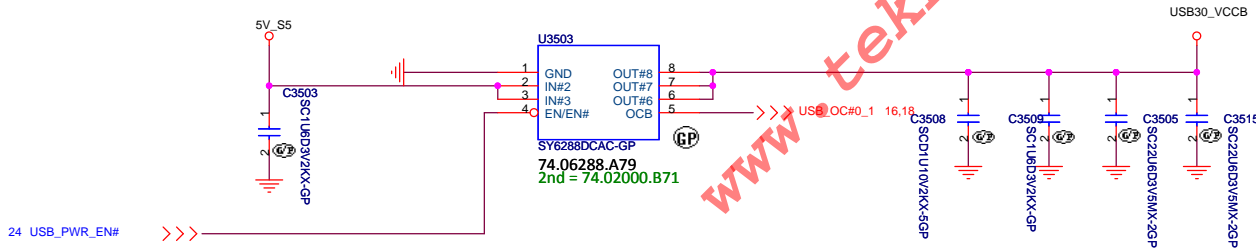
SSID = USB

For M/B USB 3.0 Power Share Port

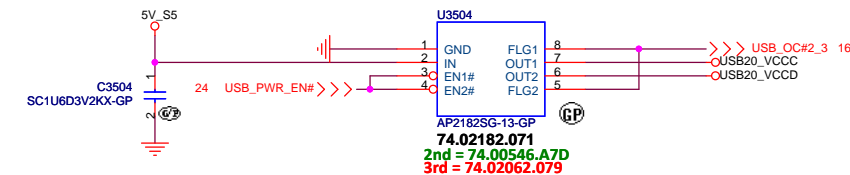


SB/ (pin 8)	SEL(pin 4)	Feature	pin 1 role (INT or INT/)
0	0	Auto S & C without mouse/keyboard pass through	INT or INT/
0	1	Auto S & C with mouse/keyboard pass through	INT or INT/
1	0	S0 charging with SDP only	INT or INT/
1	1	S0 charging with CDP or SDP only (depending on external device)	INT or INT/
0	M = (1/2)*V _{DD}	Test Mode, M = V _{DD} /2 = (1/2)*V _{DD}	

For M/B USB 3.0 Port



For IO Board USB 2.0 Port*2



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Title	USB Power SW		
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ROSA Run Power

3D3V_AUX_S5

R3607
100KR2J-1-GP

D1

PS_S3CONTROL

Q3603

1 2 3 4 5 6

D2

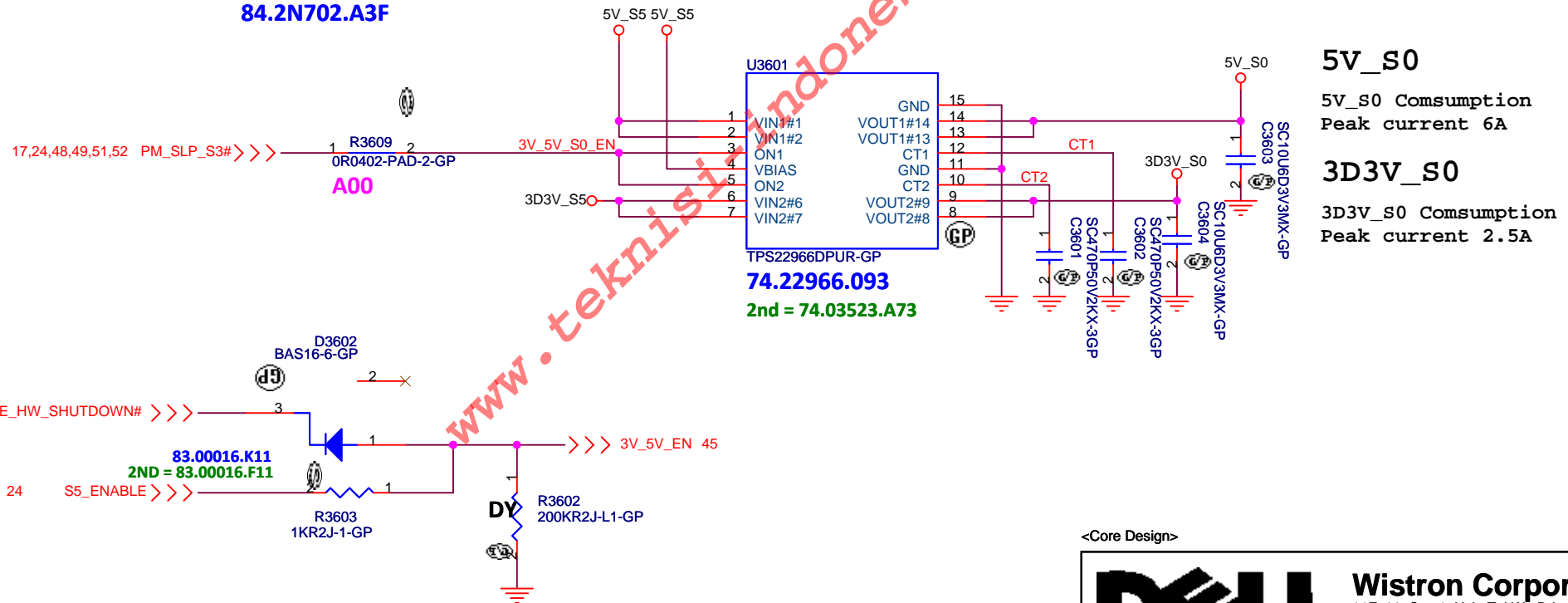
D3

2N7002KDW-GP

84.2N702.A3F

17,24,48,49,51,52 PM_SLP_S3# >>>

17,24,26 PCH_PWROK >>>



5V_S0

5V_S0 Consumption
Peak current 6A

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

<Core Design>



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Power Plane Enable

Rev
A00

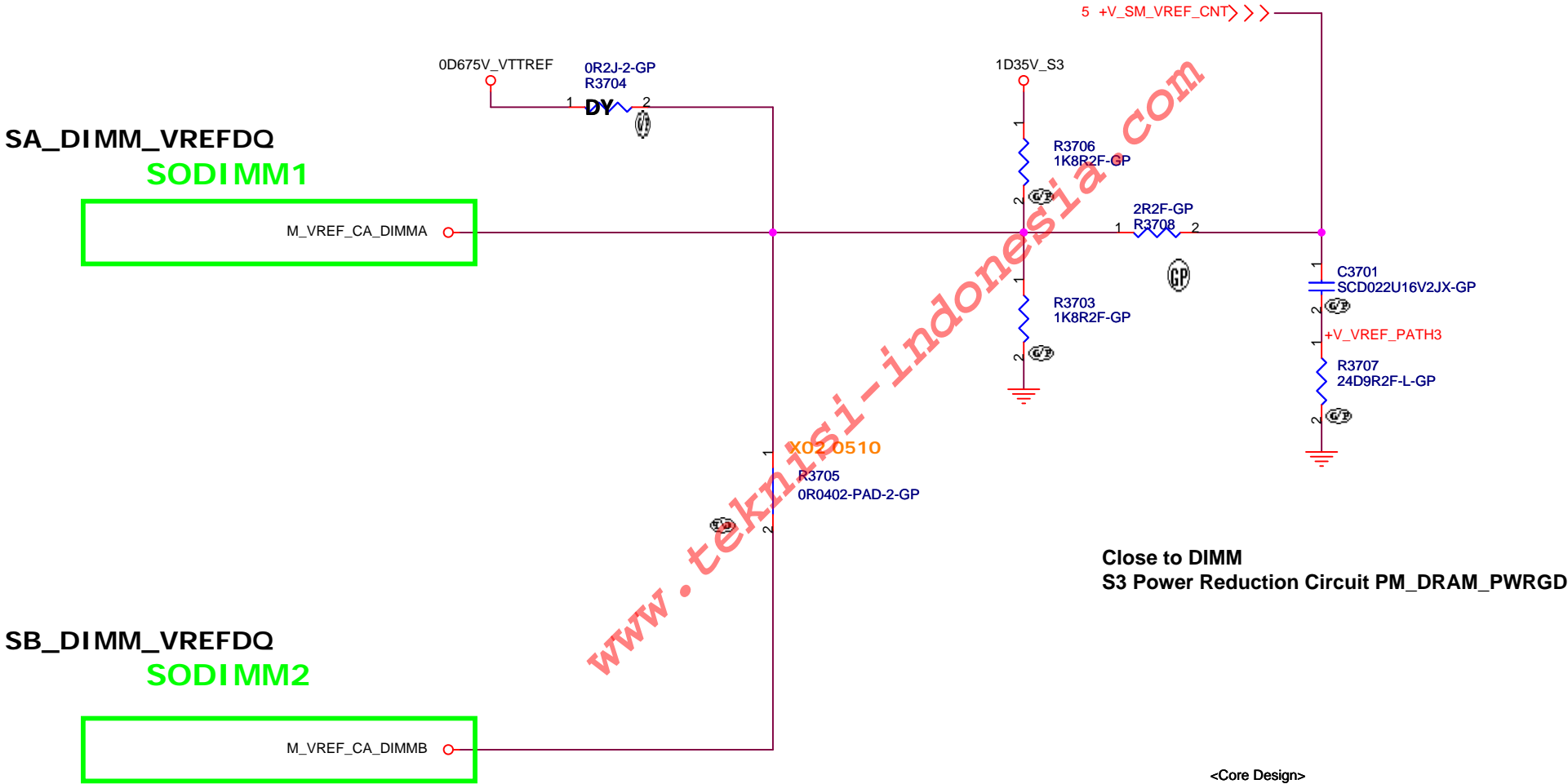
Hadley 17" MLK

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SSID = Reset.Suspend

Layout Note:

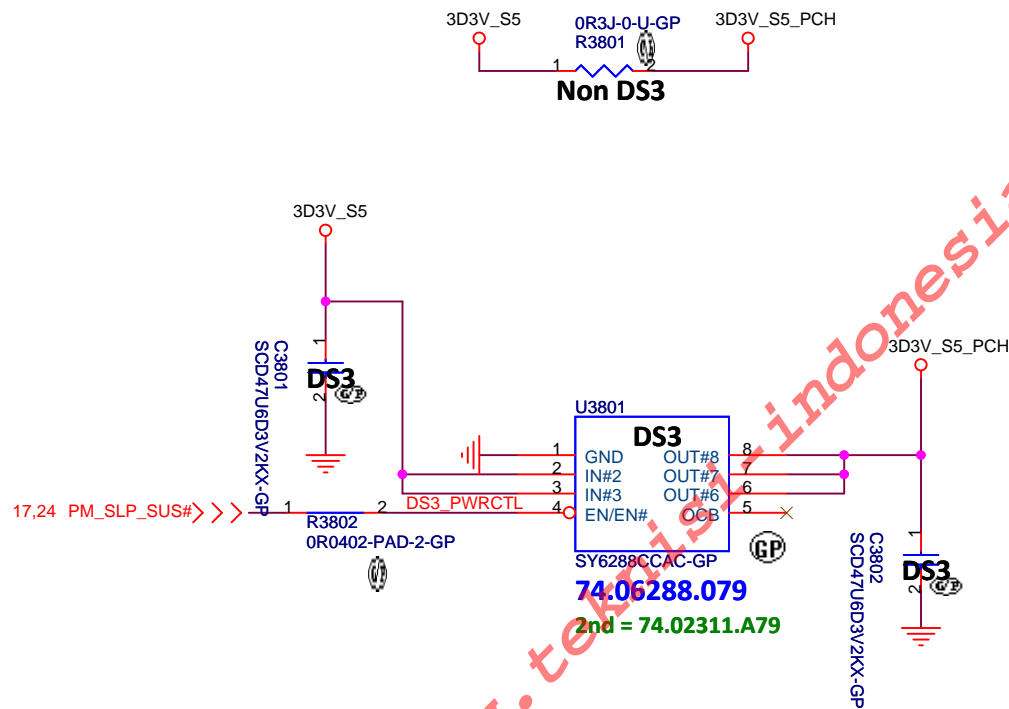
Place Close SO-DIMMA.



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title S3 Power Reduction			
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SSID = DS3



<Core Design>



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Title

DSW

Size
A4

Document Number

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Title

Reserved

Size
A3

Document Number

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Title

Reserved

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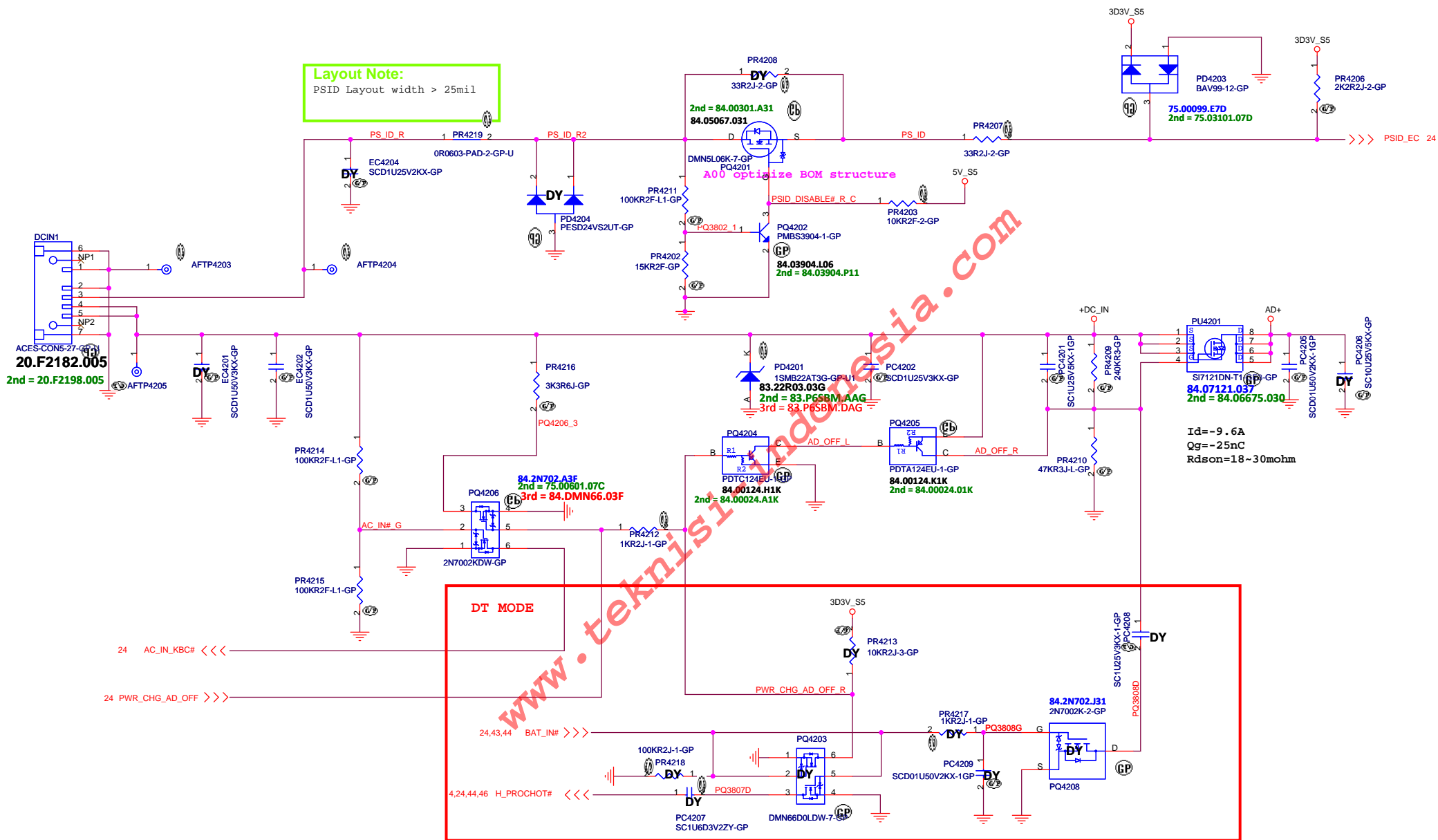
Title

Reserved

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SSID = PWR.Support



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Title

DCIN

Size

Document Number

Hadley 17" MLK

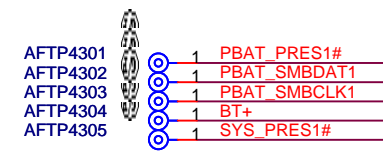
Rev

A00

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The diagram shows three identical USB-to-UART modules connected in series. Each module consists of a diode (PD4303 BAV99-12-GP), a resistor (75.00099.E7D), and another resistor (75.03101.07D). The modules are connected to BAT_IN#, BAT_SDA, and BAT_SCL lines. The output is labeled 3D3V_AUX_KBC.



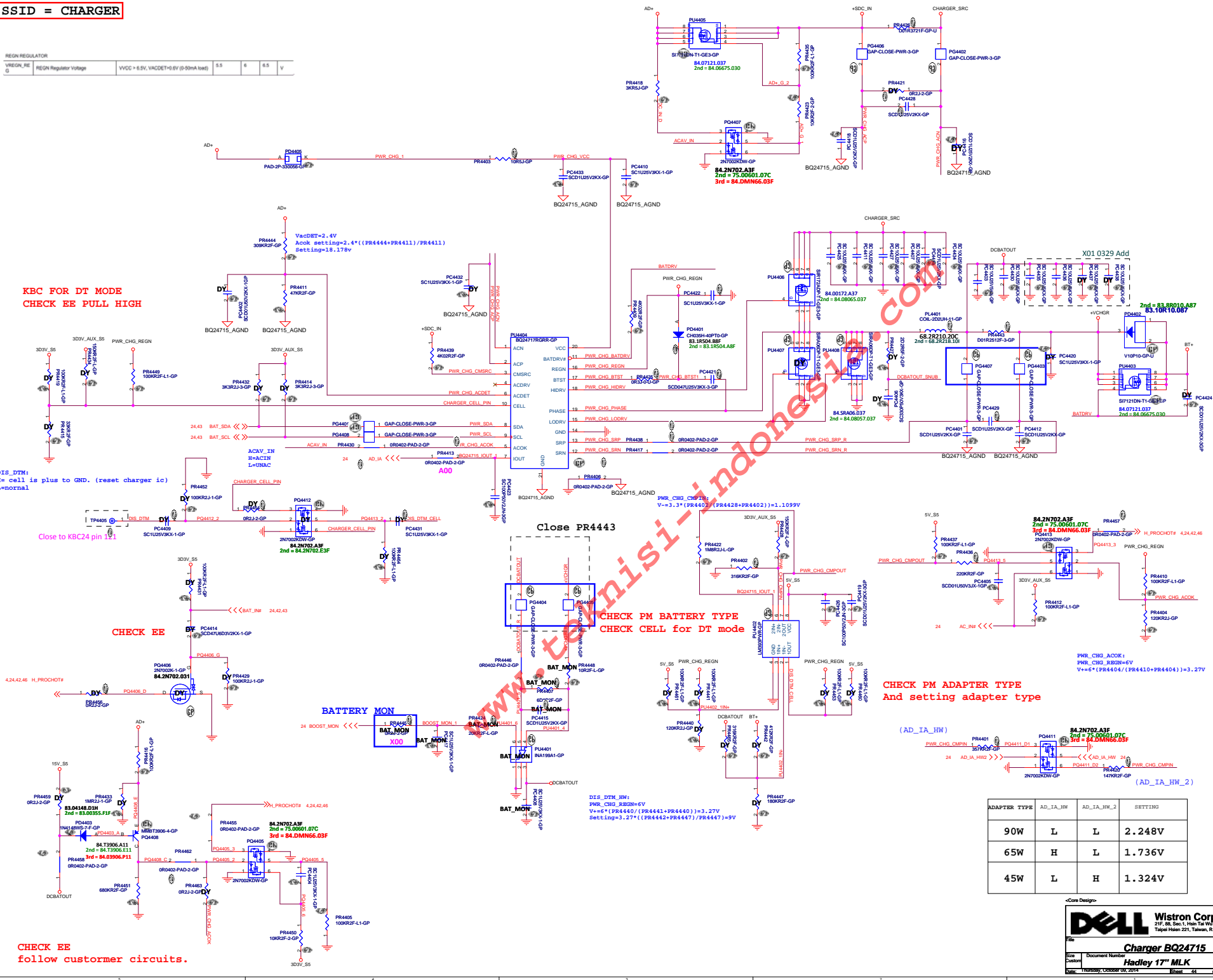
<Core Design>



Title			
BATT CONN			
Size A4	Document Number Hadley 17" MLK		Rev A00
Date:	Thursday, October 09, 2014	Sheet 43 of	103

SSID = CHARGER

REGN REGULATOR					
VREGN_RE	REGN Regulator Voltage	VVCC = 6.5V, VACDET=0.5V (0-50mA load)	5.5	6	6.5
5					



KBC FOR DT MODE
CHECK EE PULL HIGH

DIS_DTM:
H= cell is plus to GND. (reset charger ic)
L=normal

Close to KBC24 pin 12

CHECK EE

BATTERY MON

CHECK PM BATTERY TYPE
CHECK CELL for DT mode

CHECK PM ADAPTER TYPE
And setting adapter type

CHECK EE
follow customer circuits.

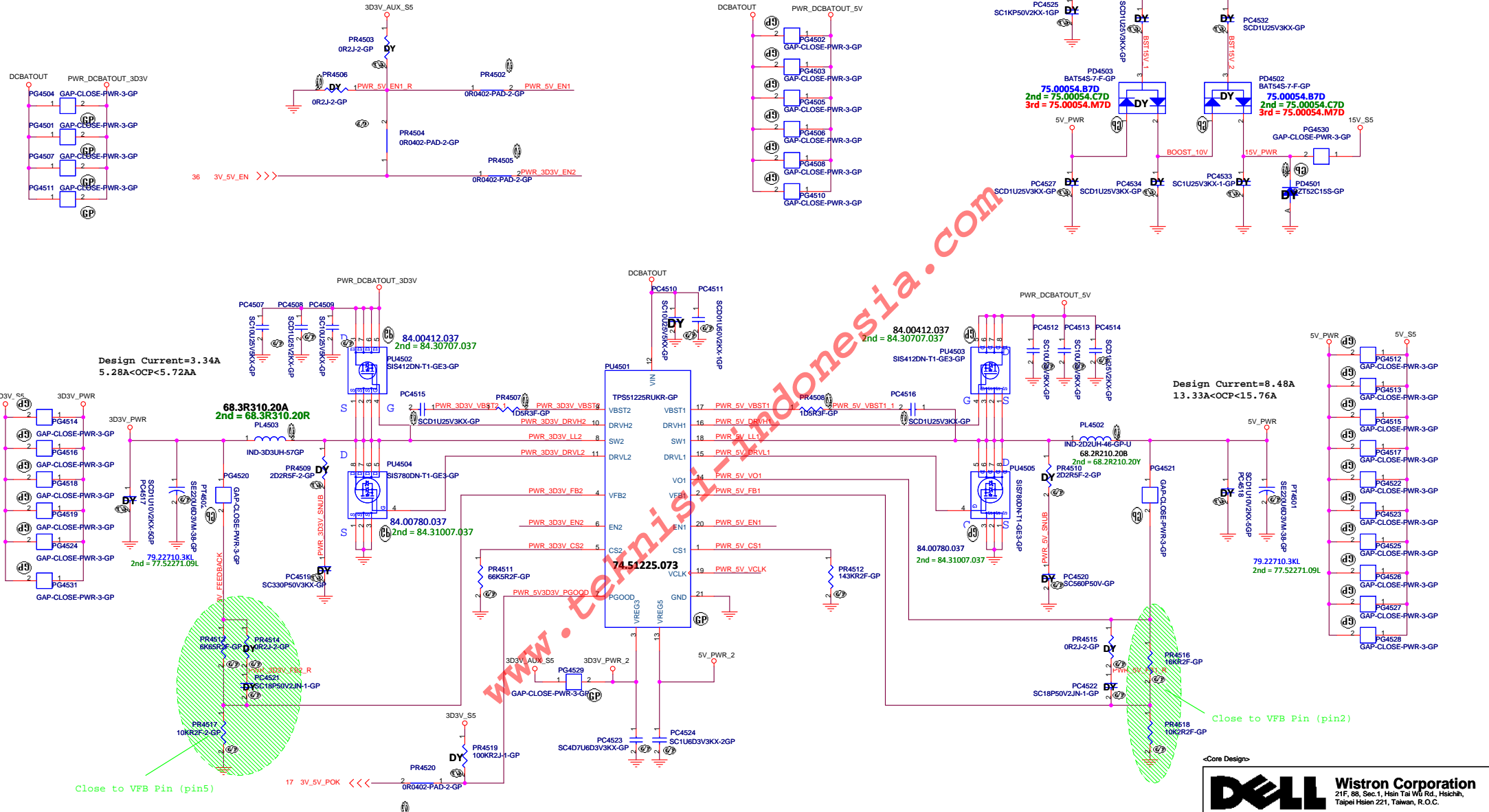
ADAPTER TYPE	AD_IA_HW	AD_IA_HW_2	SETTING
90W	L	L	2.248V
65W	H	L	1.736V
45W	L	H	1.324V

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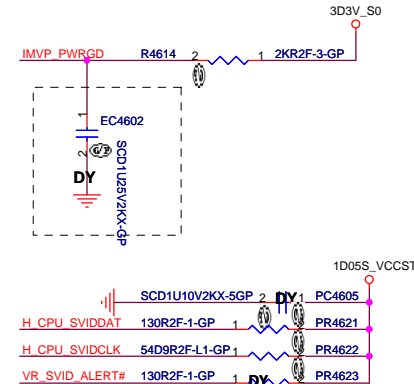
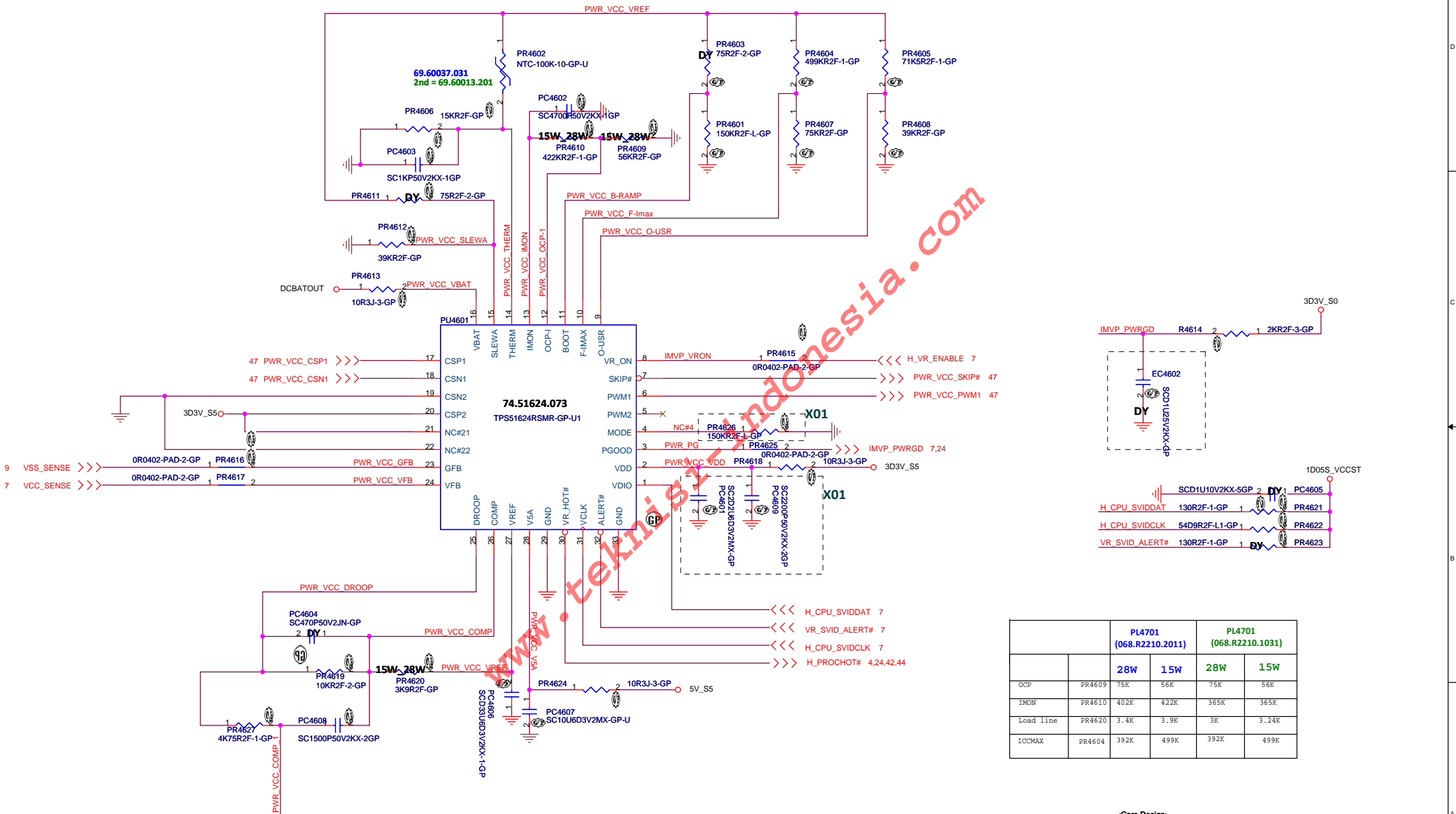
Charger BQ24715

Size	Document Number	Rev
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SSID = PWR.Plane.Regulator_5v3p3v



SSID = CPU.Regulator



		PL4701 (068.R2210.2011)		PL4701 (068.R2210.1031)	
		28W	15W	28W	15W
OC	PR4609	75K	56K	75K	56K
IMON	PR4610	402K	422K	365K	365K
Load line	PR4620	3.4K	3.9K	3K	3.24K
IOCMAX	PR4604	392K	499K	392K	499K

<Core Design>

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Title

046P TPS51624 CPUCORE(1/2)

Size A3

Document Number

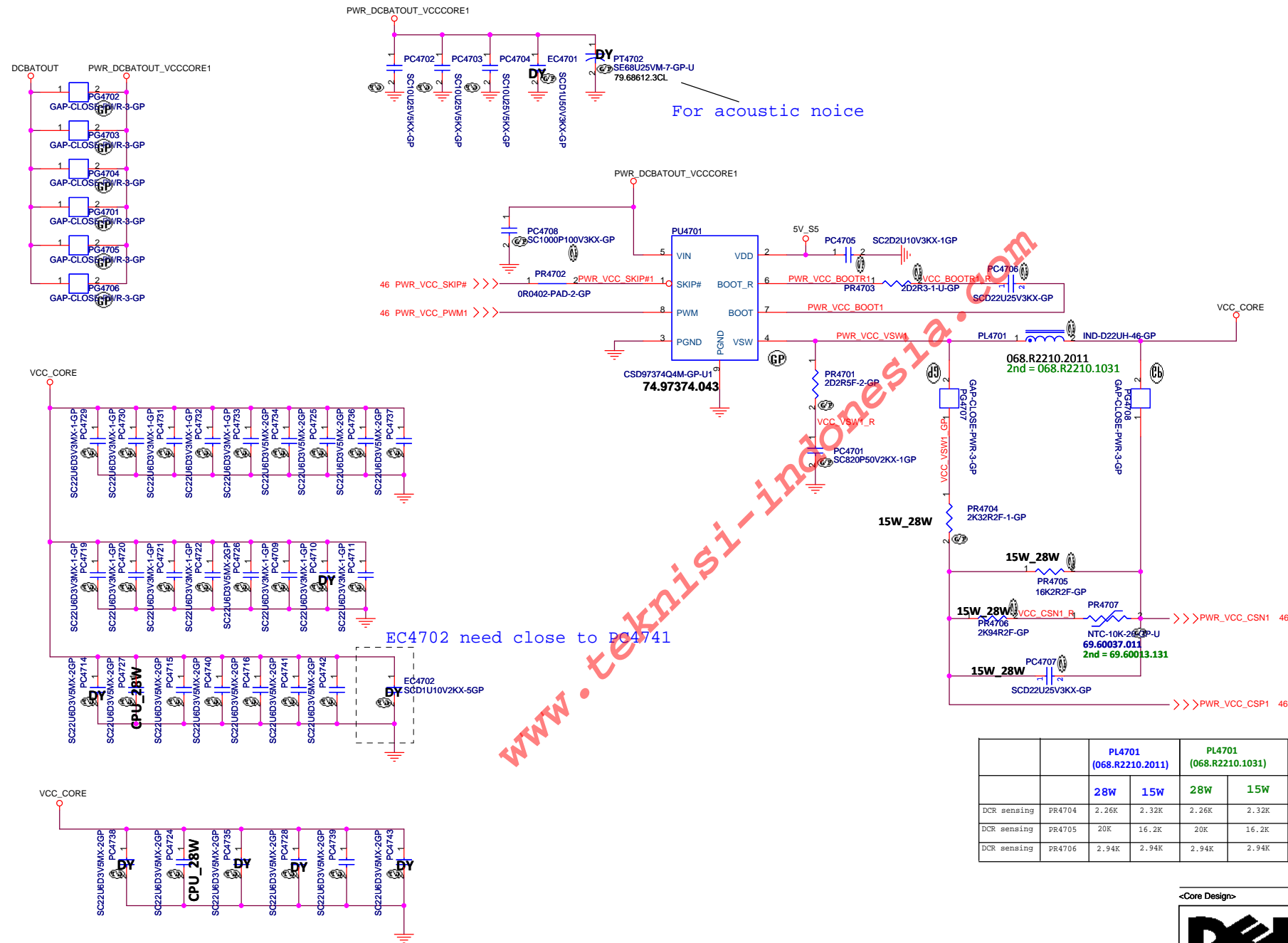
Hadley 17" MLK

Date: Thursday, October 09, 2014

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Rev **A00**

SSID = CPU.Regulator



		PL4701 (068.R2210.2011)		PL4701 (068.R2210.1031)	
		28W	15W	28W	15W
DCR sensing	PR4704	2.26K	2.32K	2.26K	2.32K
DCR sensing	PR4705	20K	16.2K	20K	16.2K
DCR sensing	PR4706	2.94K	2.94K	2.94K	2.94K

<Core Design>



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Title

047P TPS51624 CPUCORE(2/2)

Size	A3
------	----

Document Number

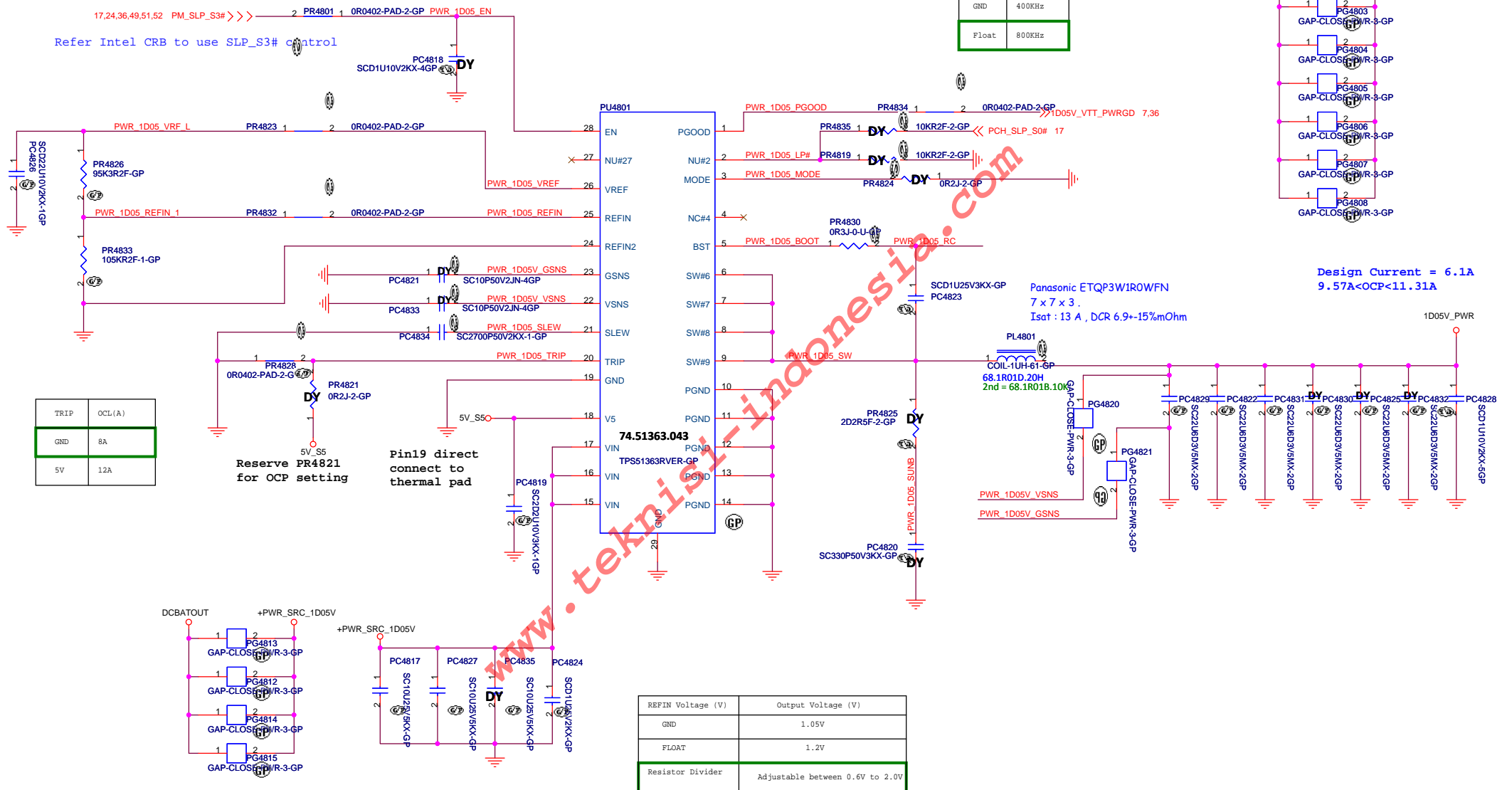
Hadley 17" MLK

Rev
X02

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```
SSID = PWR.Plane.Regulator_1p05v
```



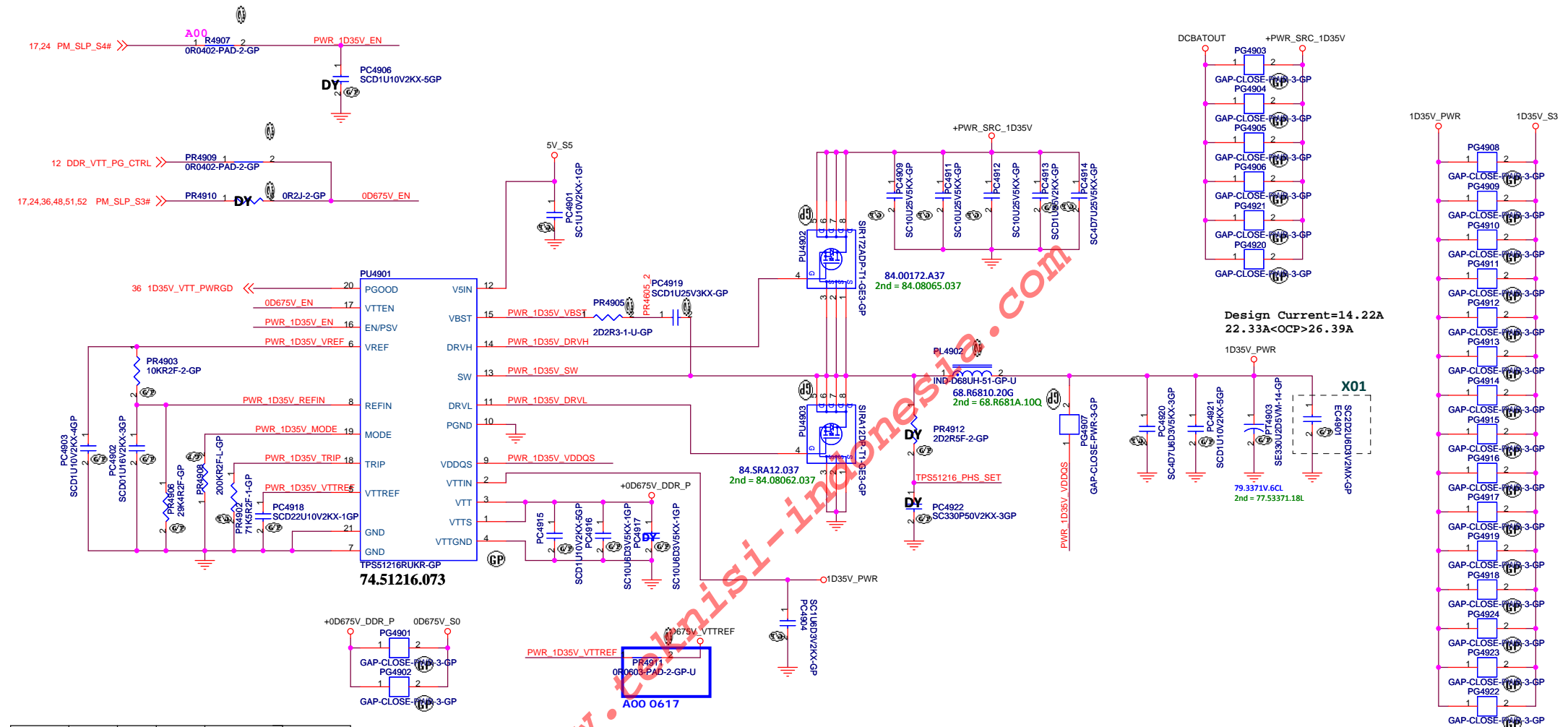
I/P cap: CHIP CAP C 100 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 1.0UH ETQP3W1R0WFN / Panasonic/ 6.9mOhm / Isat =13Arms/ 68.1R01D.20H
O/P cap:CHIP CAP C 22U 6.3V M0805 X5L /78.22610.51L

<Core Design>



Title			
TPS51363 1D05V			
Size A3	Document Number		Rev
	Hadley 17" MLK		A00
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SSID = PWR.Plane.Regulator 1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE		
PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 1.0UH PCMB104T-1ROM/ 3.3mohm/ Isat =28A rms /68.1R01C.10Q
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S: SIR172ADP-T1-GE3 / 8.5mohm/10.5mOhm/4.5Vgs/ 84.00172.A37
L/S: SIRA12DP-T1-GE3 / 4.4mohm/6mOhm/4.5Vgs/ 84.SRA12.037

<Core Design>




Title			
TPS51367/51206 1D35V/0D675V			
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Title

(Reserved)TPS51312 1D8V

Size
A3

Document Number
Hadley 17" MLK

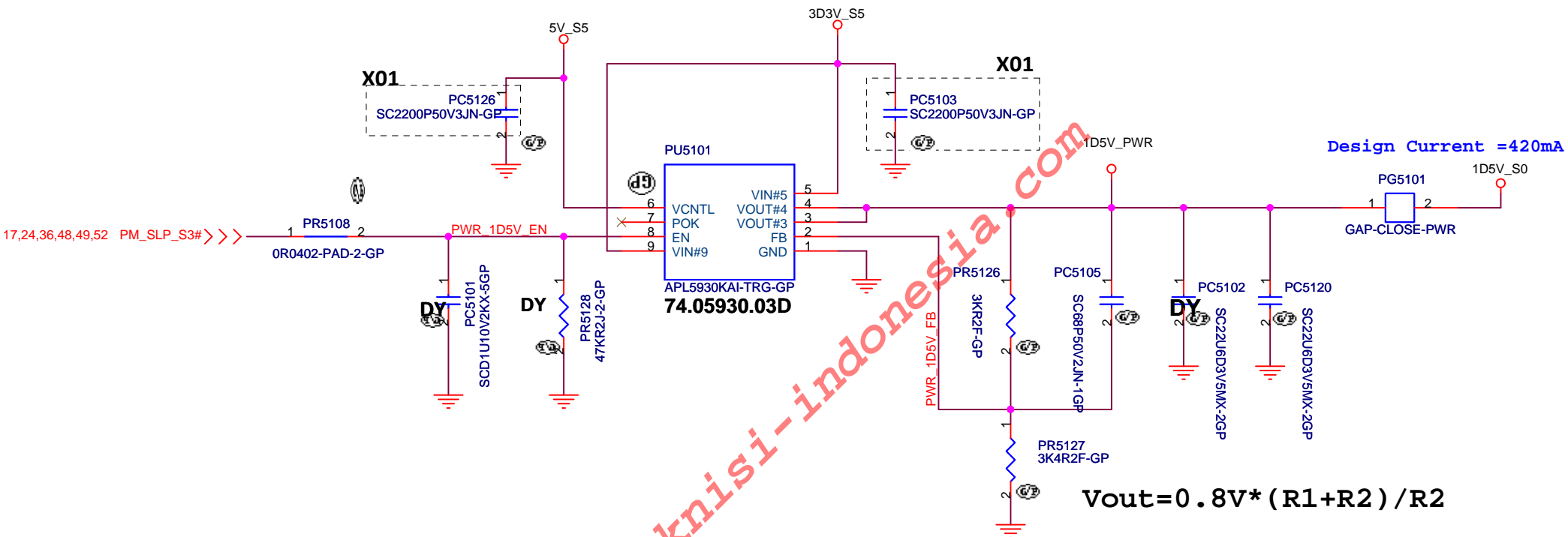
Date: Friday, September 19, 2014

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SSID = PWR.Plane.Regulator_1p5v

APL5930KAI for 1D5V_S0



$$V_{out} = 0.8V * (R1 + R2) / R2$$


<Core Design>

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Title APL5930 1D5V			
Size A4	Document Number Hadley 17" MLK		Rev X02
Date: Thursday, October 09, 2014		Sheet 51	of 103

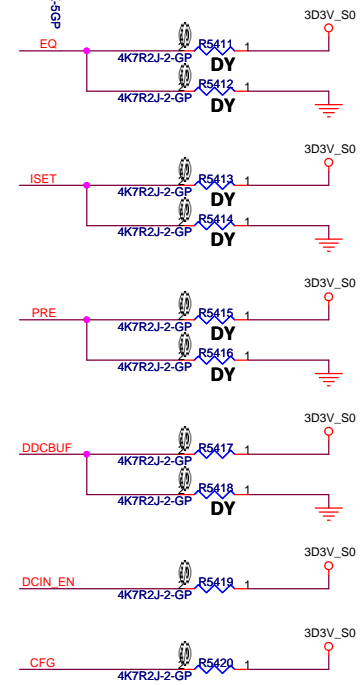
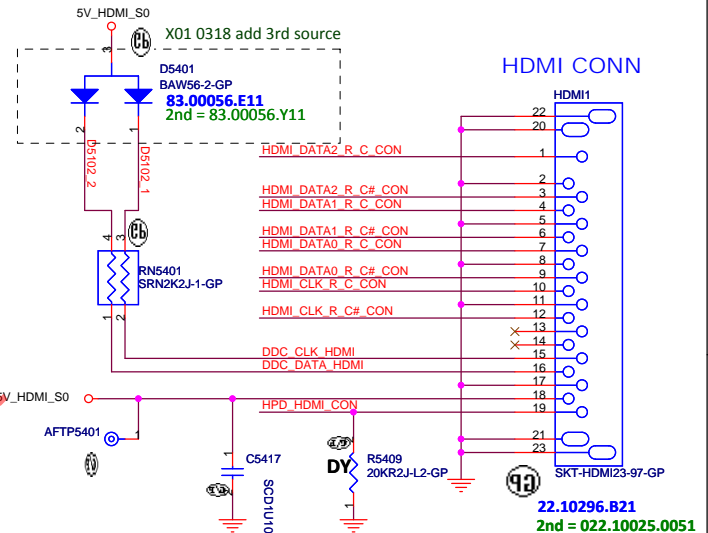
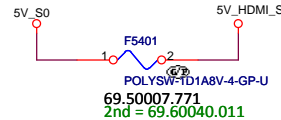
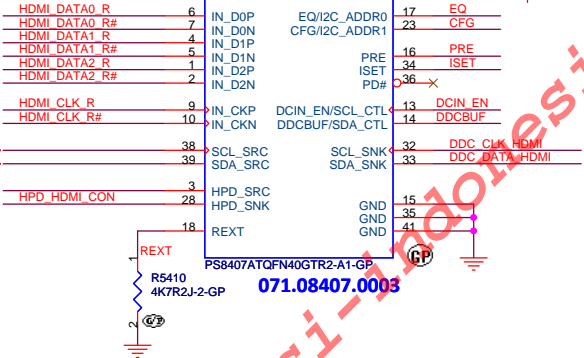
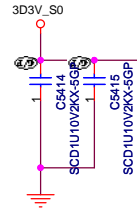
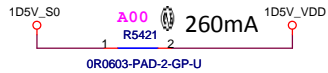
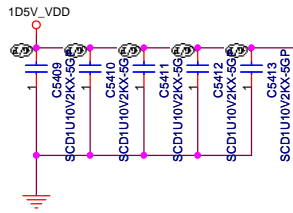
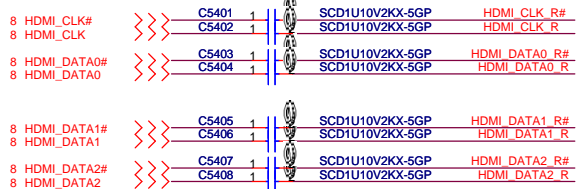
(Blanking)

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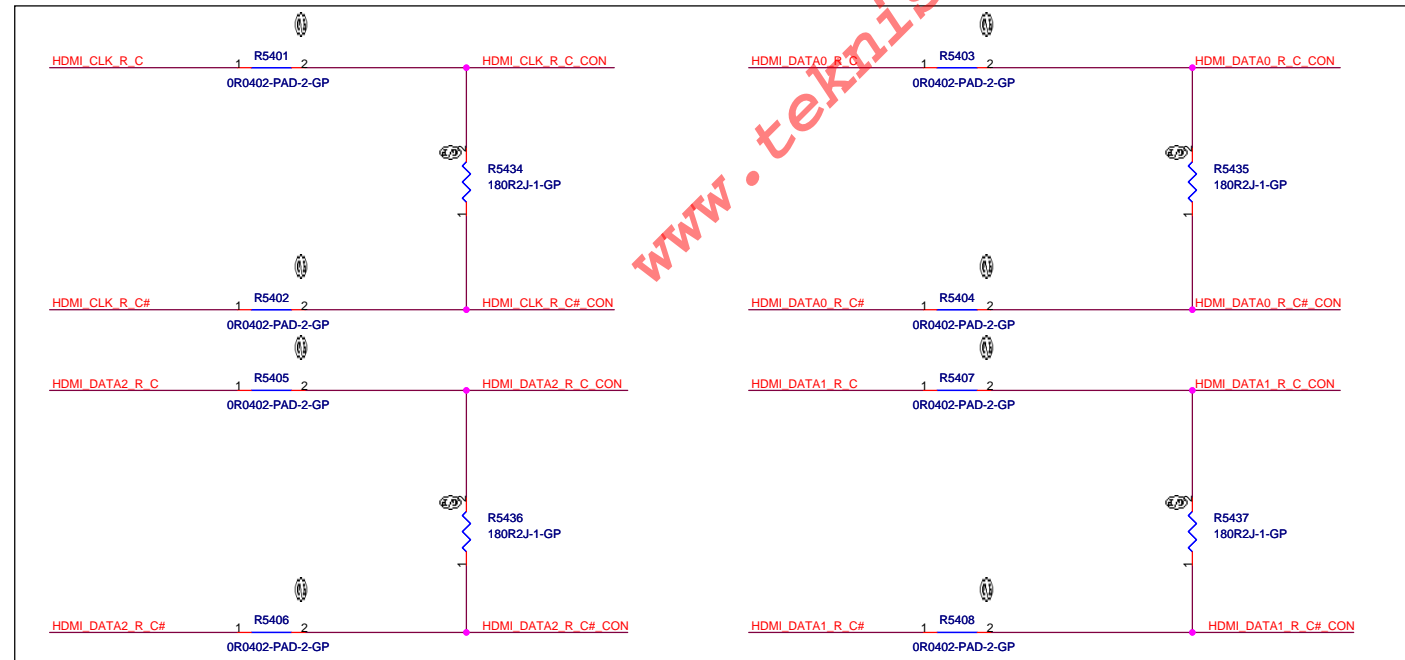
<Core Design>

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Title			
LVDS Switch			
Size	Document Number		Rev
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SSID = VIDEO



A00 remove co-layout



<Core Design>

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Title: **HDMI Repeater/Connector**
 Size A3 Document Number: **Hadley 17" MLK** Rev X02
 Date: Thursday, October 08, 2014 Sheet 54 of 103

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Title

Reserved

Size
A4

Document Number

Hadley 17" MLK

Rev
A00

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Table 1: Tx/Rx EQ & DE Pulse Width Settings

DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (default)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

ODD Connector

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Title

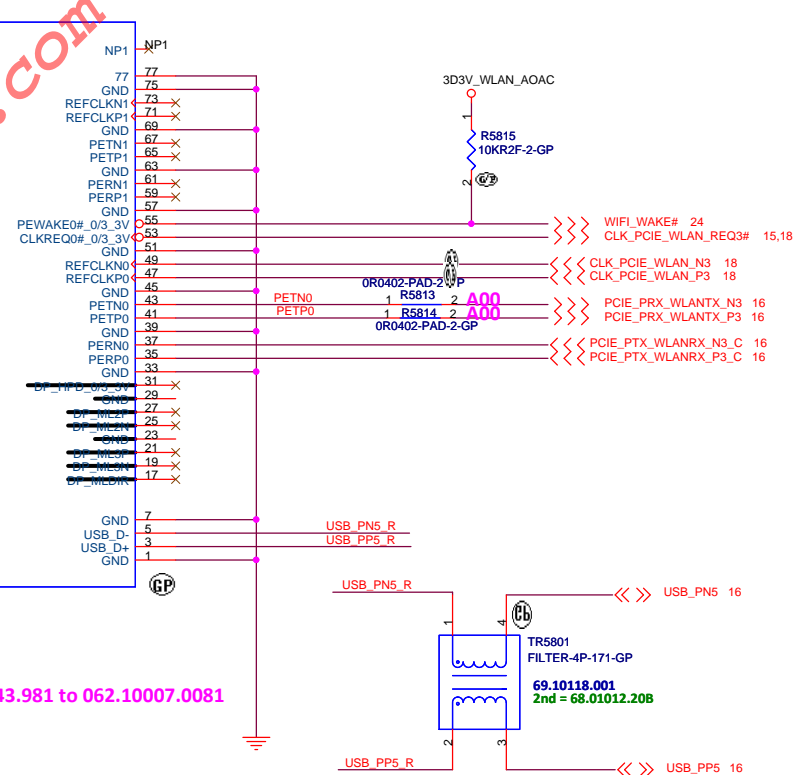
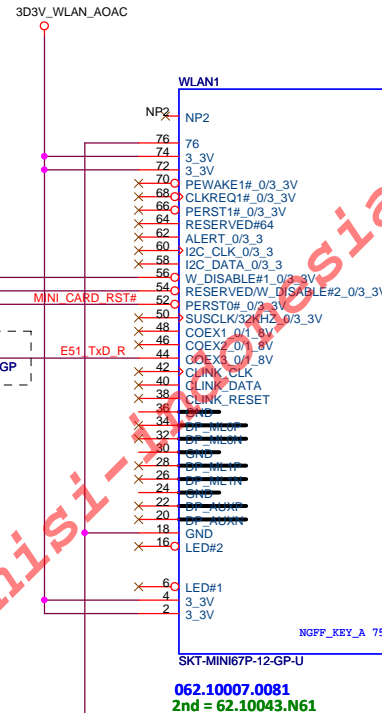
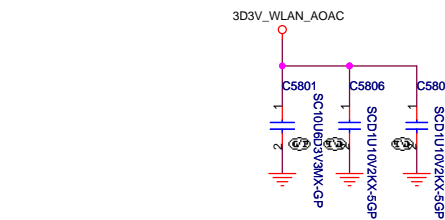
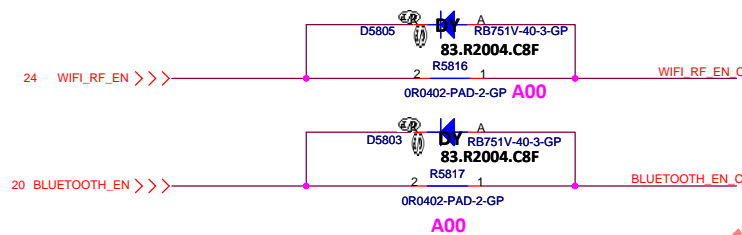
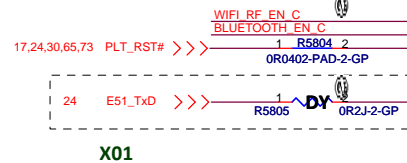
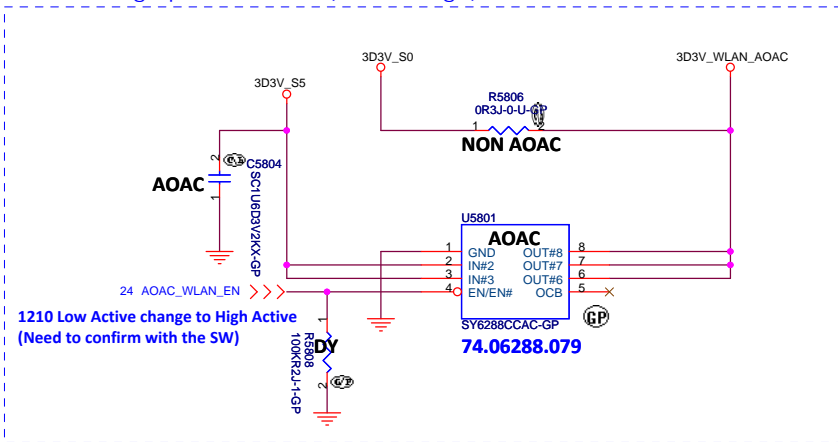
Reserved

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SSID = Wireless

1210 change power switch(Active High)




<Core Design>

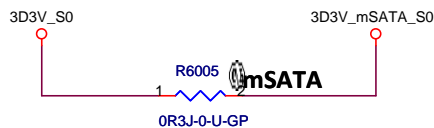
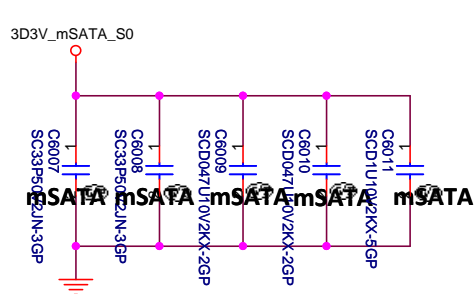
(Blanking)

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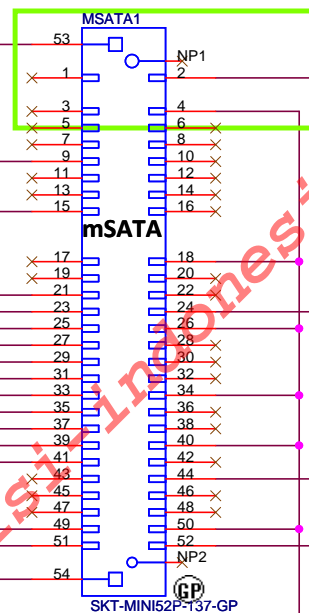
<Core Design>

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Title			
Reserved			
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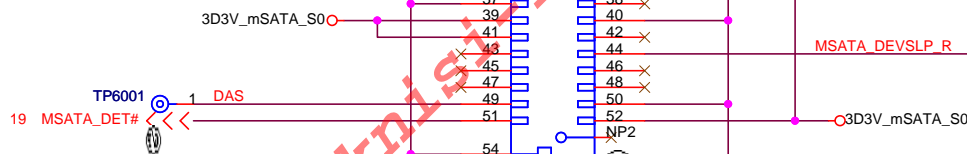
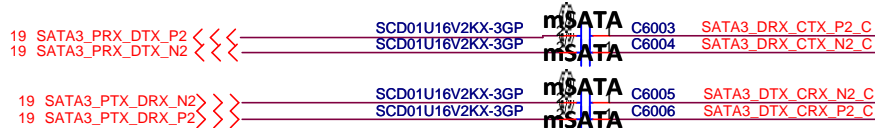
SSID = mSATA



MSATA CONN



62.10043.H01
2nd = 62.10043.G61
3rd = 20.F1693.052



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Title

mSATA

Size

Custom

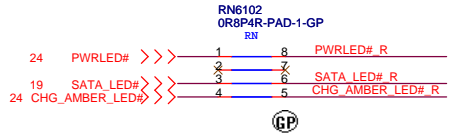
Hadley 17" MLK

Rev

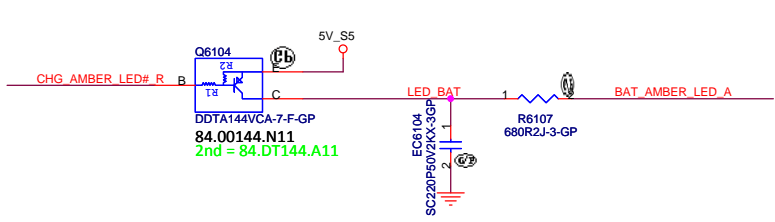
A00

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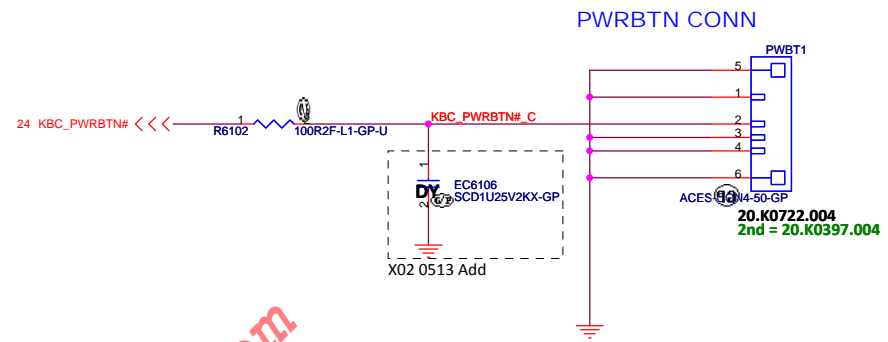
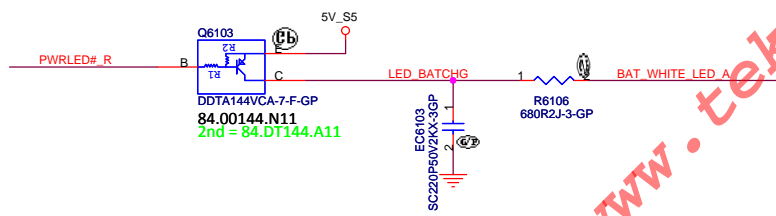
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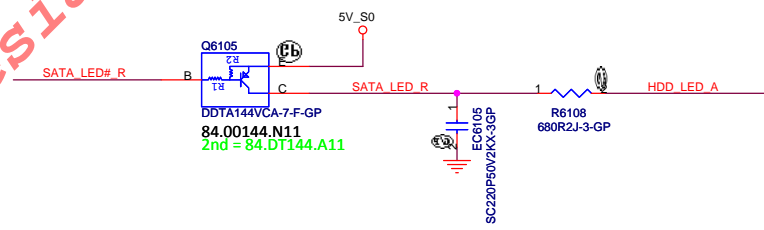
Battery LED1(Amber_LED)
LOW acted from KBC GPIO



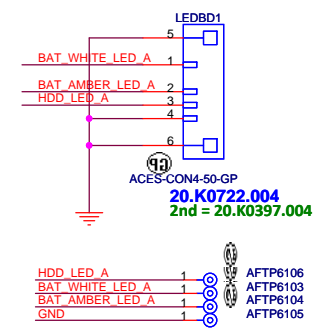
Battery LED2(White_LED)
LOW acted from KBC GPIO



SATA HDD LED
LOW acted from PCH GPIO

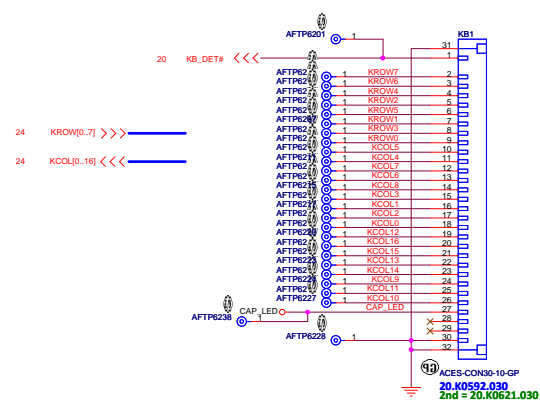


LED board CONN

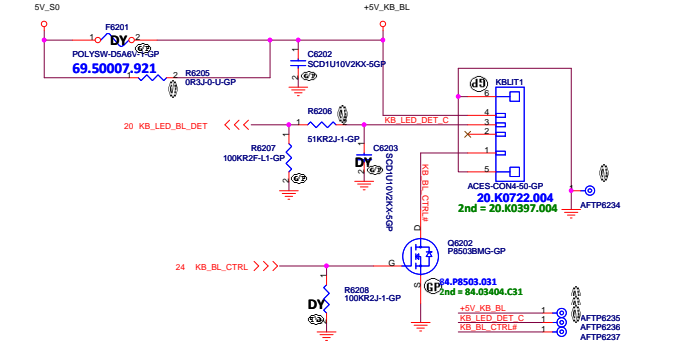
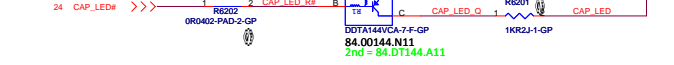


SSID = KBC

Internal Keyboard Connector

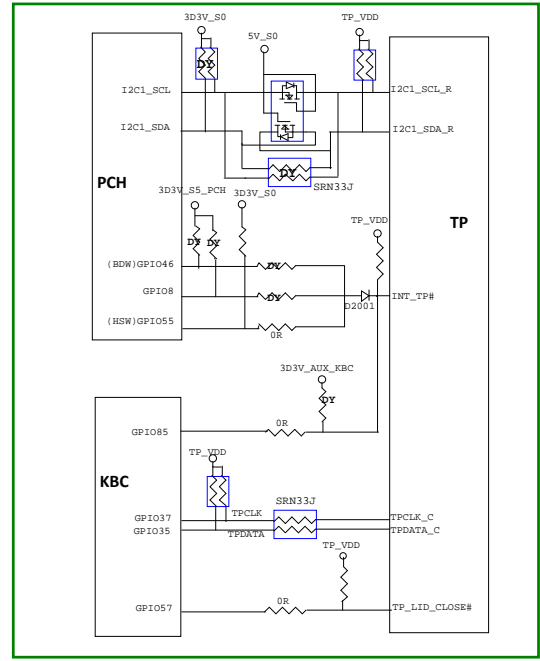
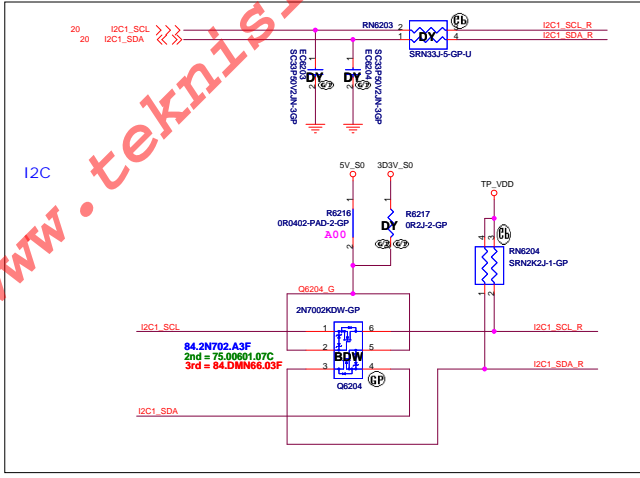
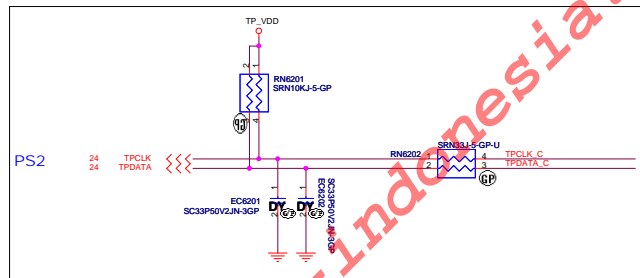
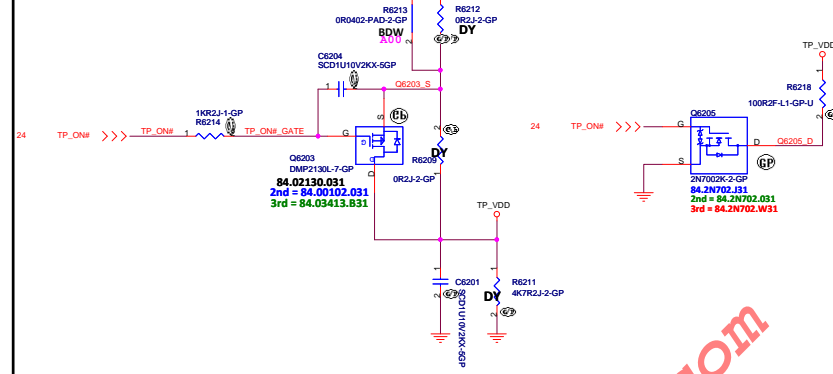


CAP LED Control
LOW acted from KBC GPIO

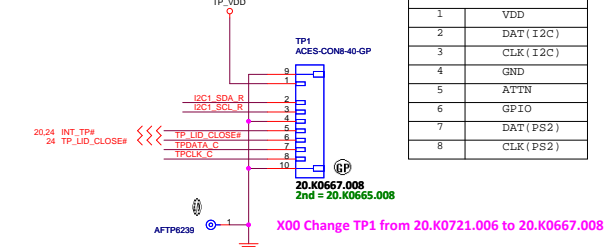


SSID = Touch.Pad

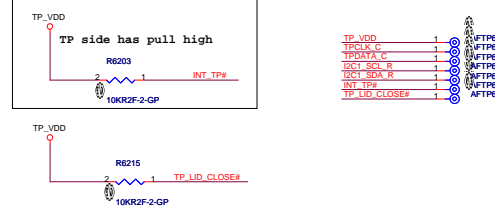
BDW: Support PTP



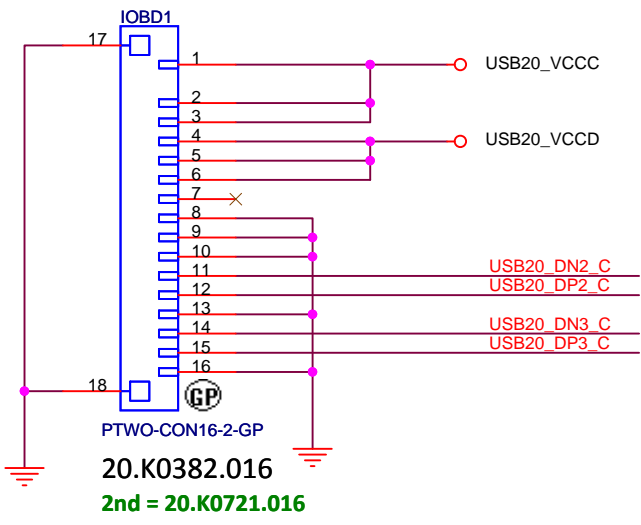
Touch Pad Connector



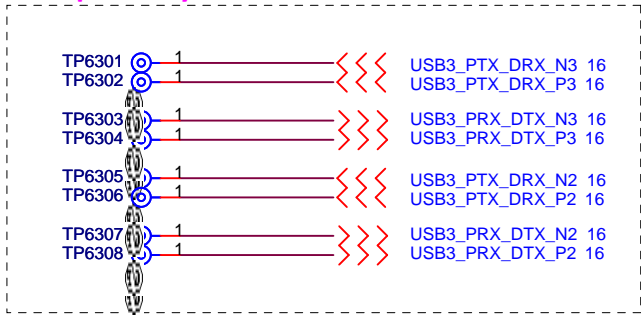
Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



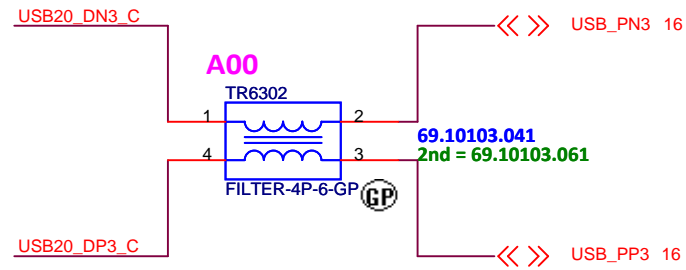
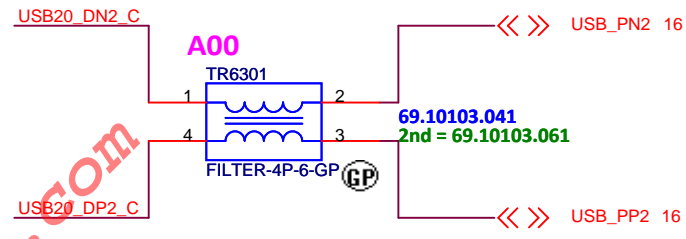
SSID = User.Interface



Keep Hadley17 USB3.0 trace



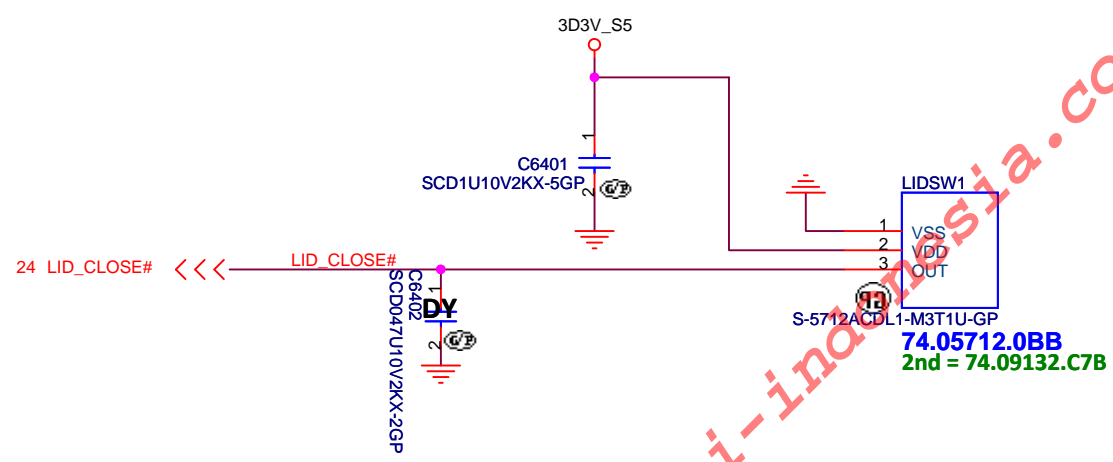
X01 0328 stuff CMC, dummy IO board CMC.




<Core Design>

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Title IO Board Connector			
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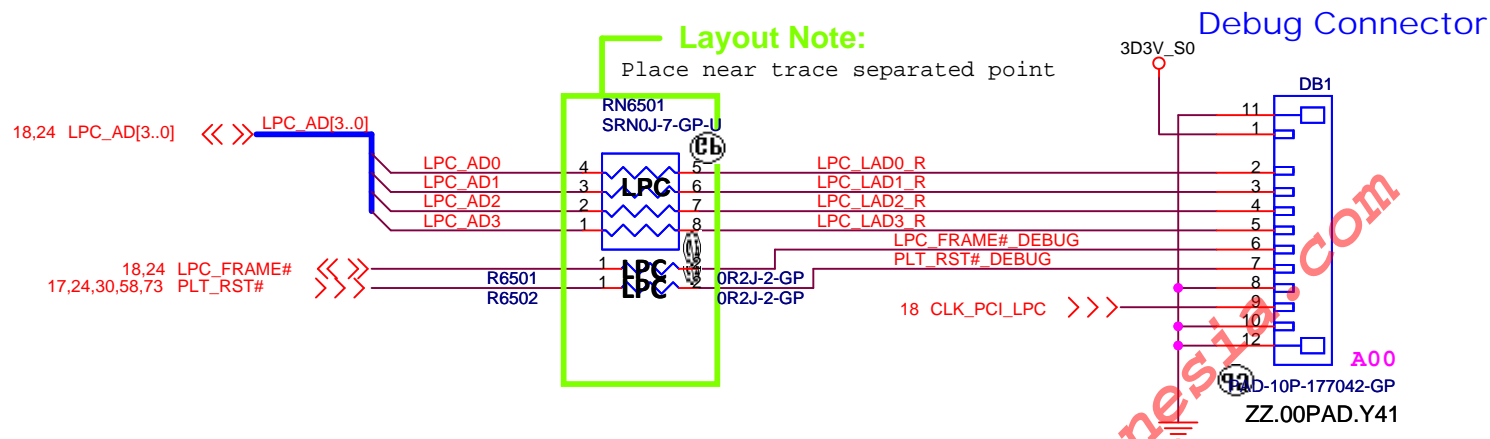
SSID = User.Interface



<Core Design>

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Title <i>Hall Sensor</i>			
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SSID = DEBUG PORT



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Title

Dubug connector

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Title

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Size
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Document Number

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(Blanking)

<Core Design>

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Title

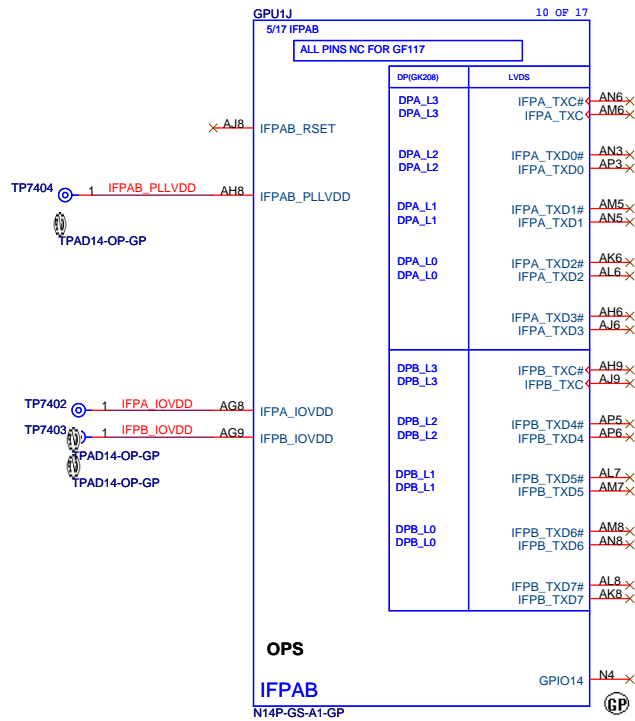
Size
A3

Document Number
Reserved
Hadley 17" MLK

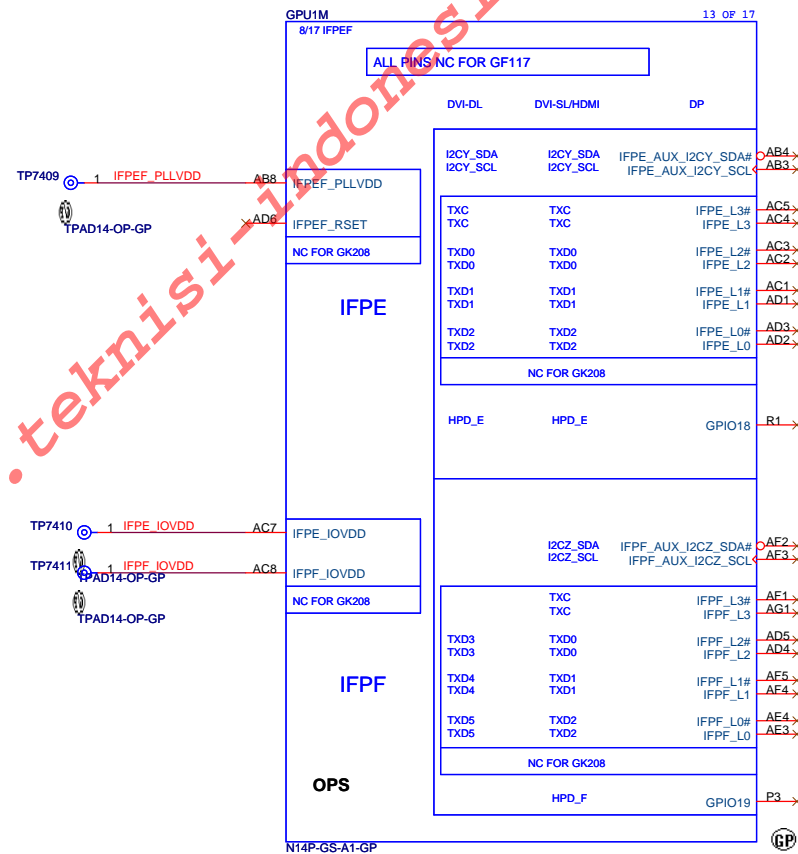
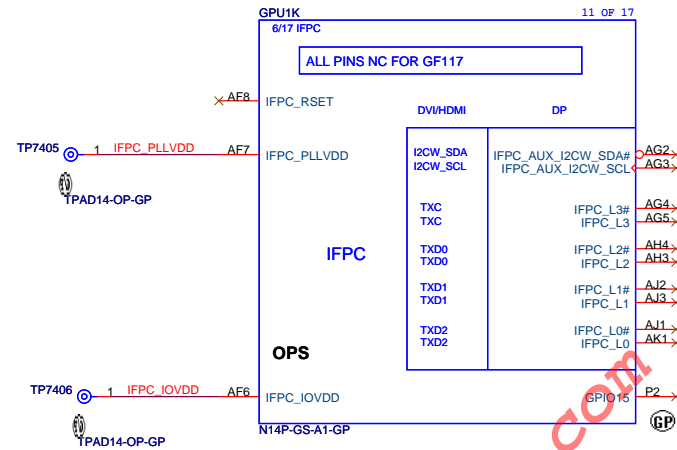
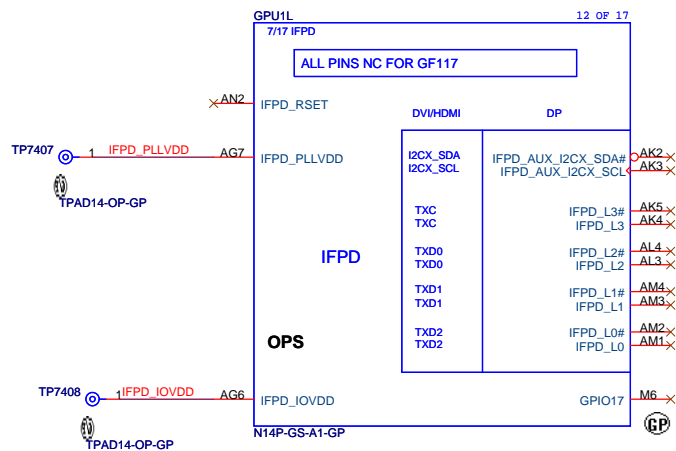
Rev
A00

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LVDS Interface



HDMI Interface

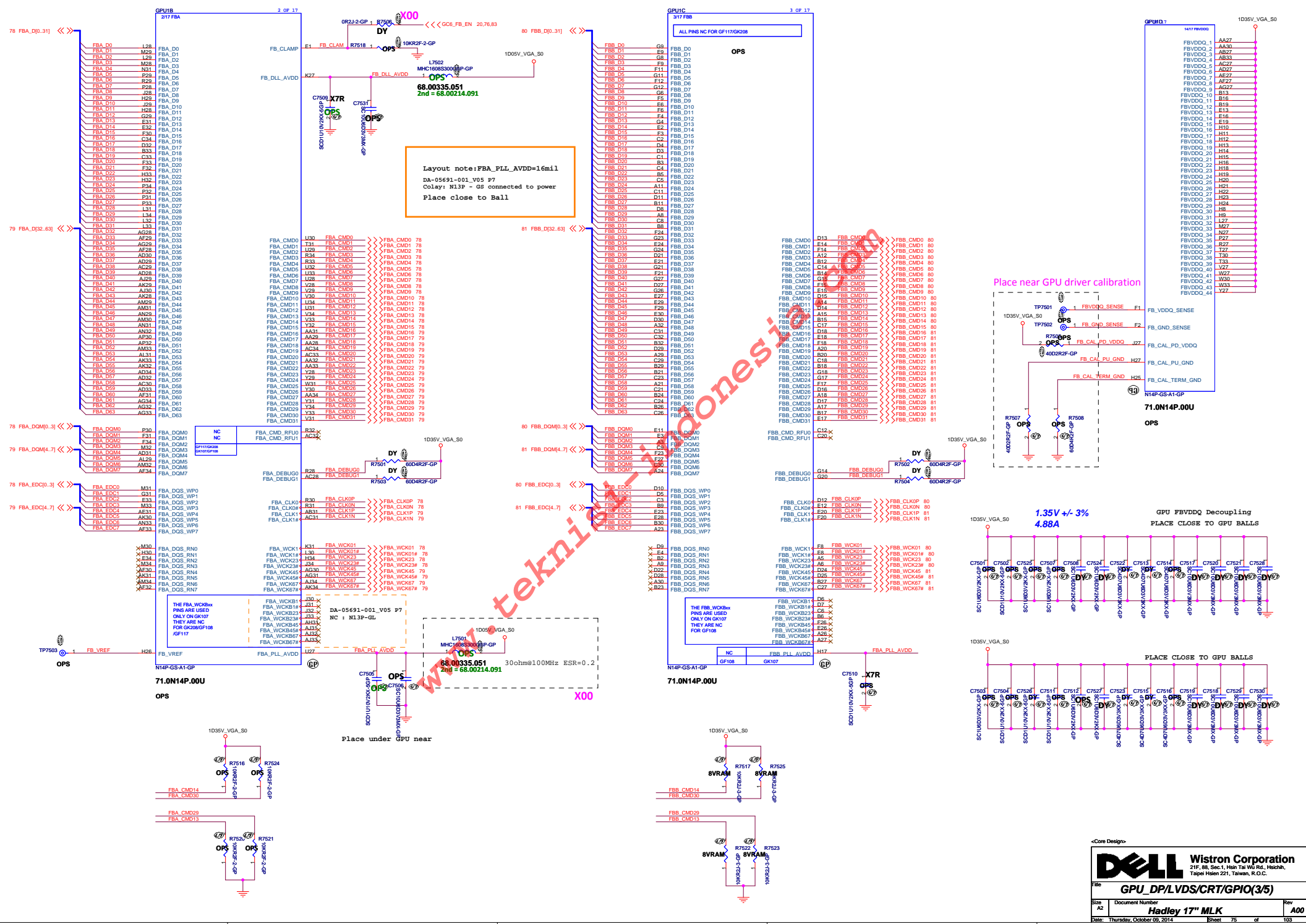


<Core Design>

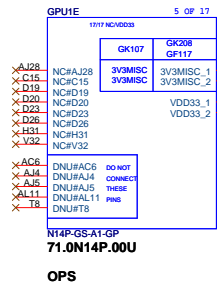
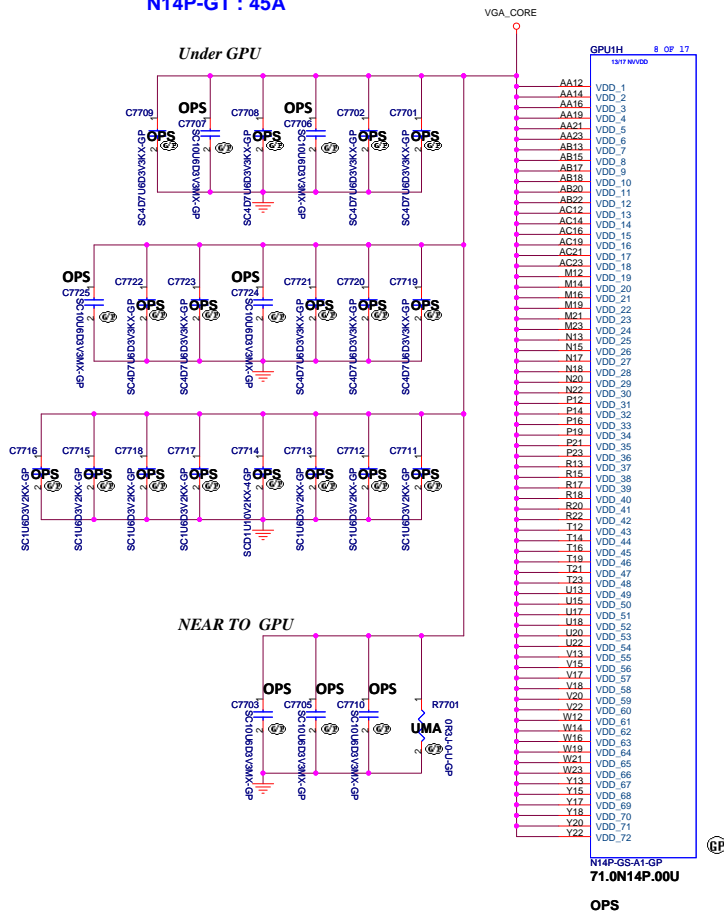


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SSID = GPU

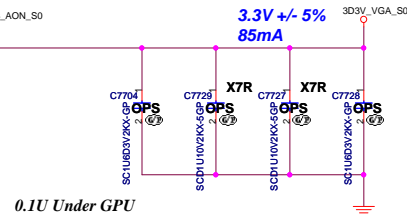


N14P-GT : 45A



X00
J8,K8

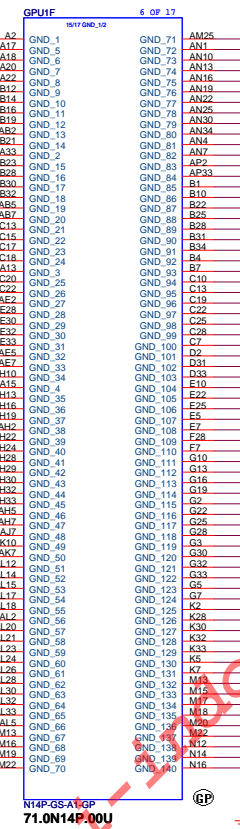
If GC6 2.0 is implemented, connect to a 3V3 rail that will be on in GC6.
If GC6 2.0 is NOT implemented, connect to the same rail as VDD33.



0.1U Under GPU

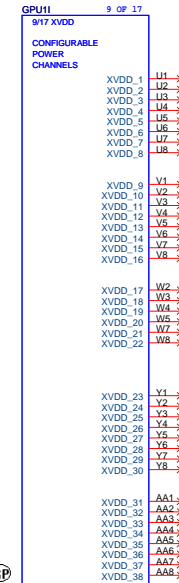
4.7U NEAR TO GPU

1U NEAR TO GPU



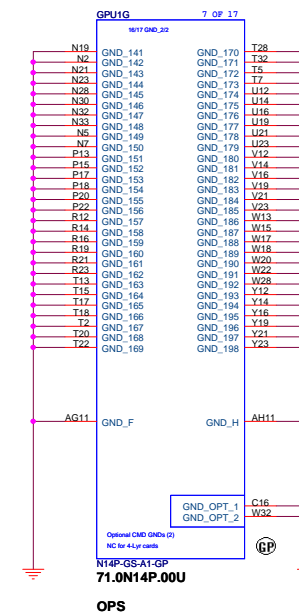
N14P-GS-A1-GP
71.0N14P.00U

OPS



N14P-GS-A1-GP
71.0N14P.00U

OPS

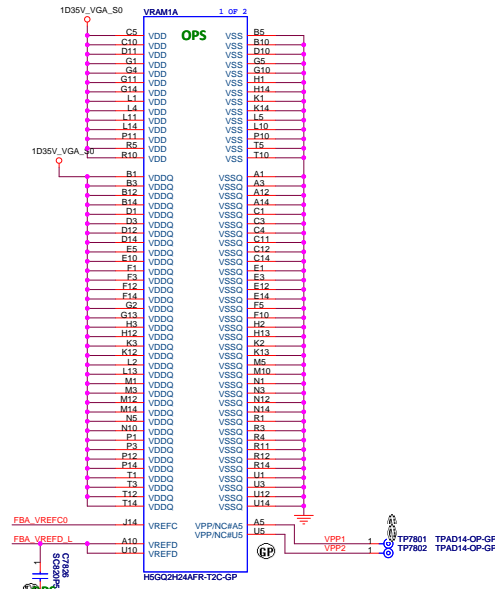


XVDD_1~38
NC : N13P-GL

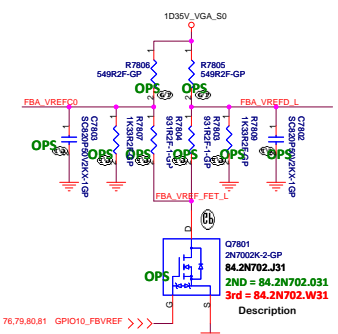
<Core Design>



SSID = VRAM

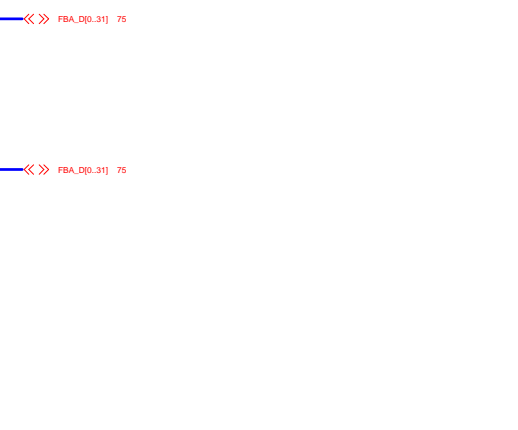
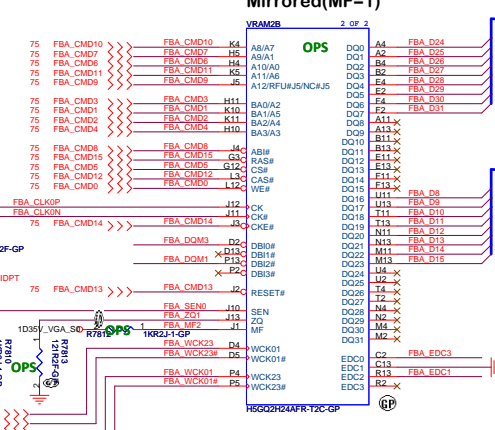
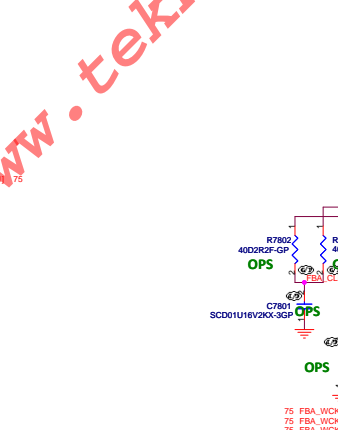
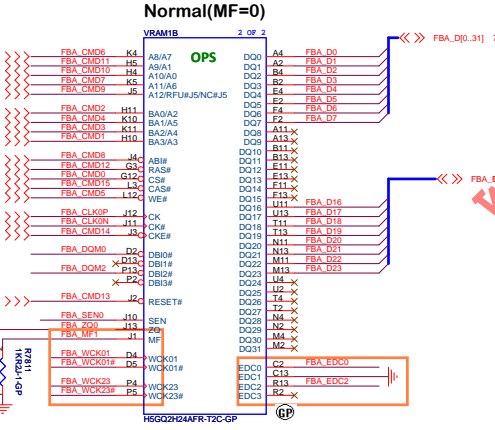
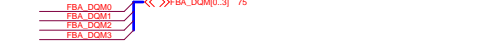
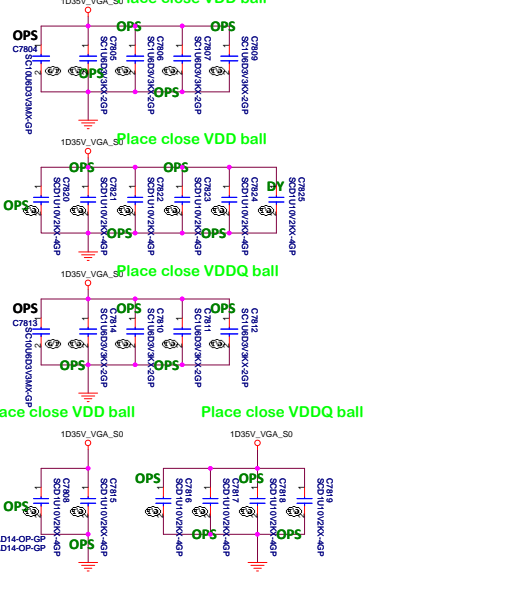
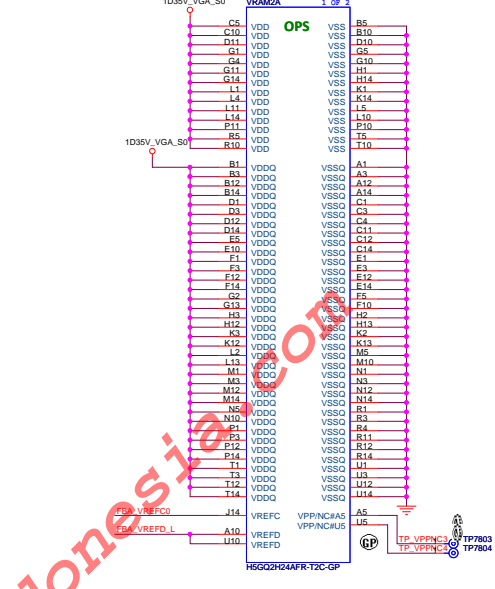


Frame Buffer Partition A-Lower Half

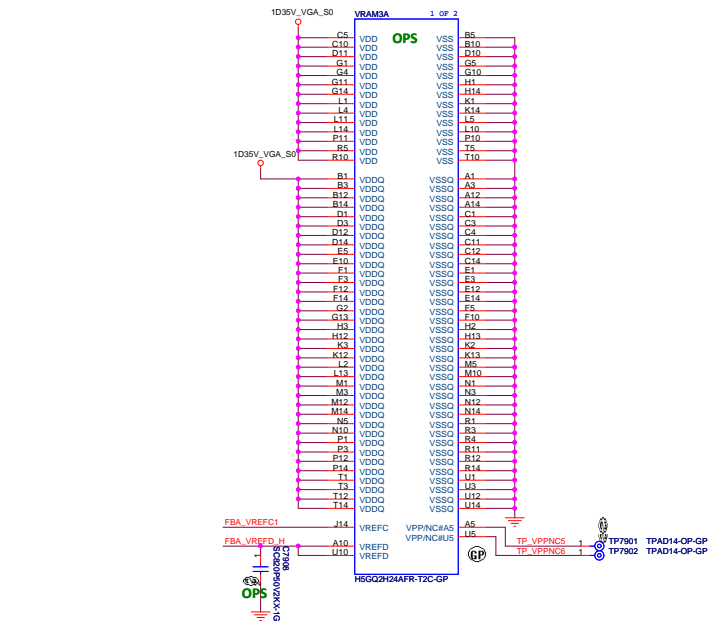


FBVREF Termination

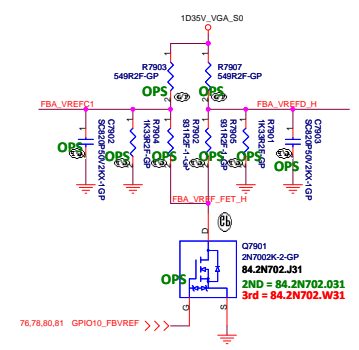
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



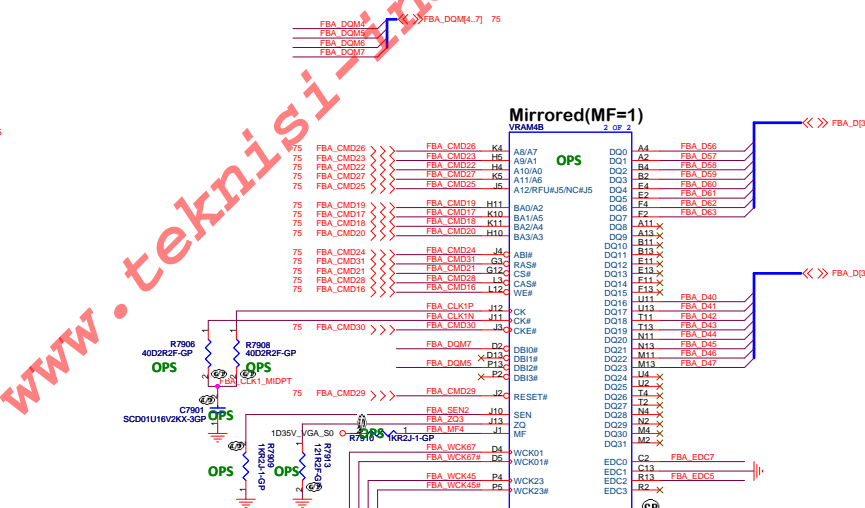
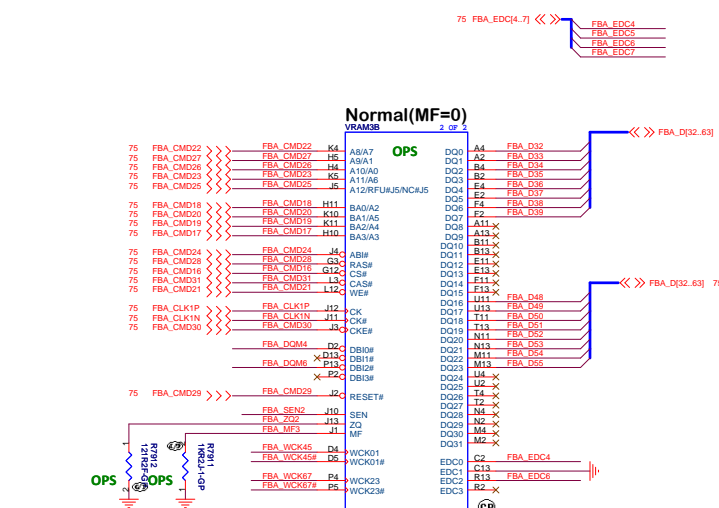
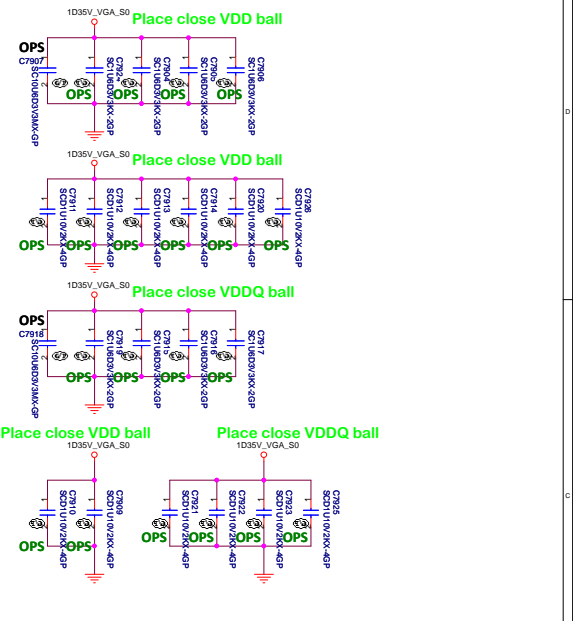
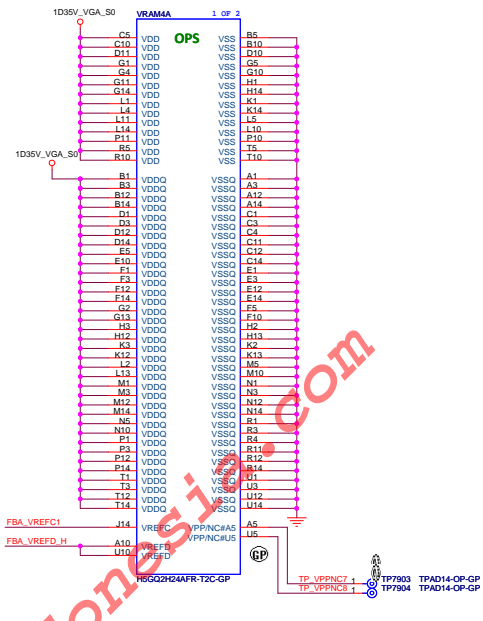
SSID = VRAM

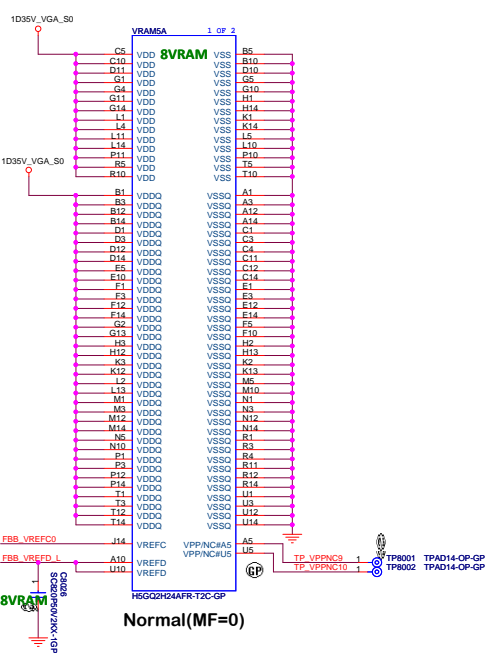


Frame Buffer Partition A-Upper Half

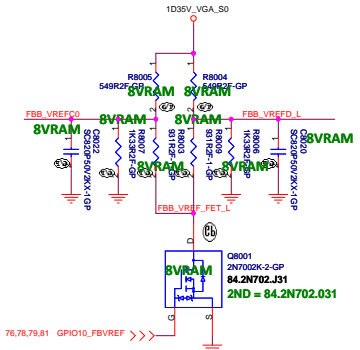


Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



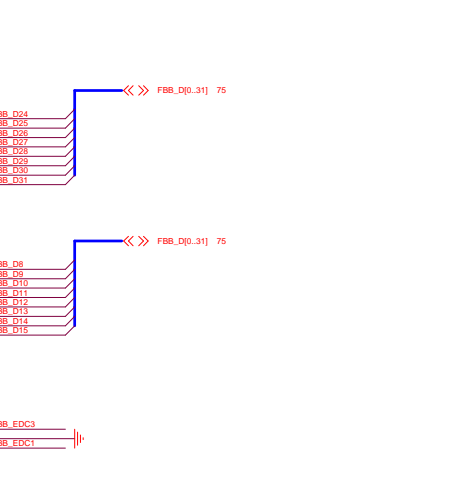
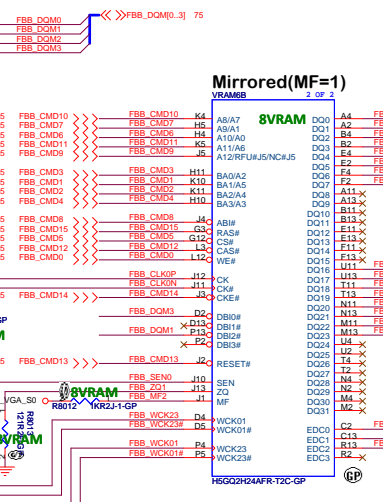
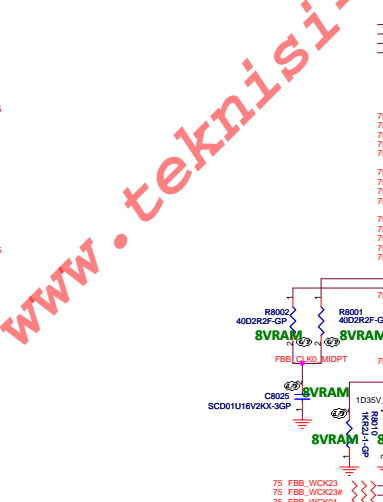
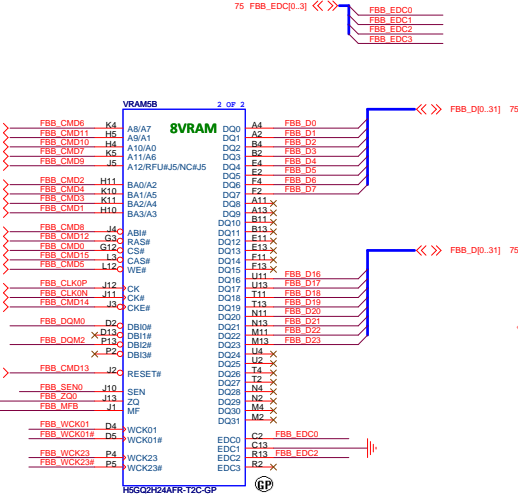
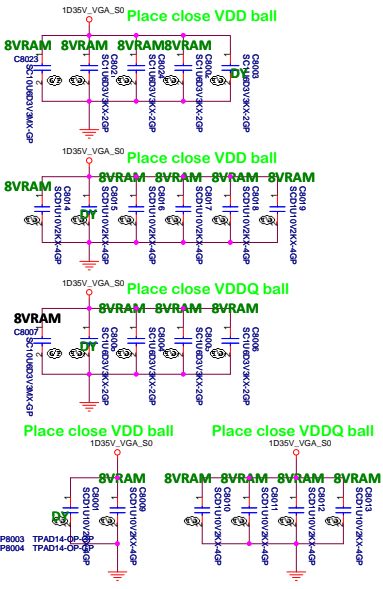
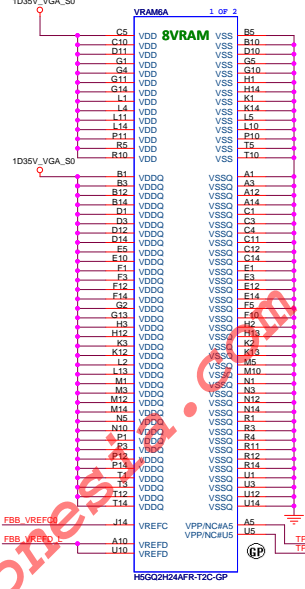


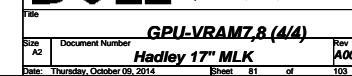
Frame Buffer Partition B-Lower Half



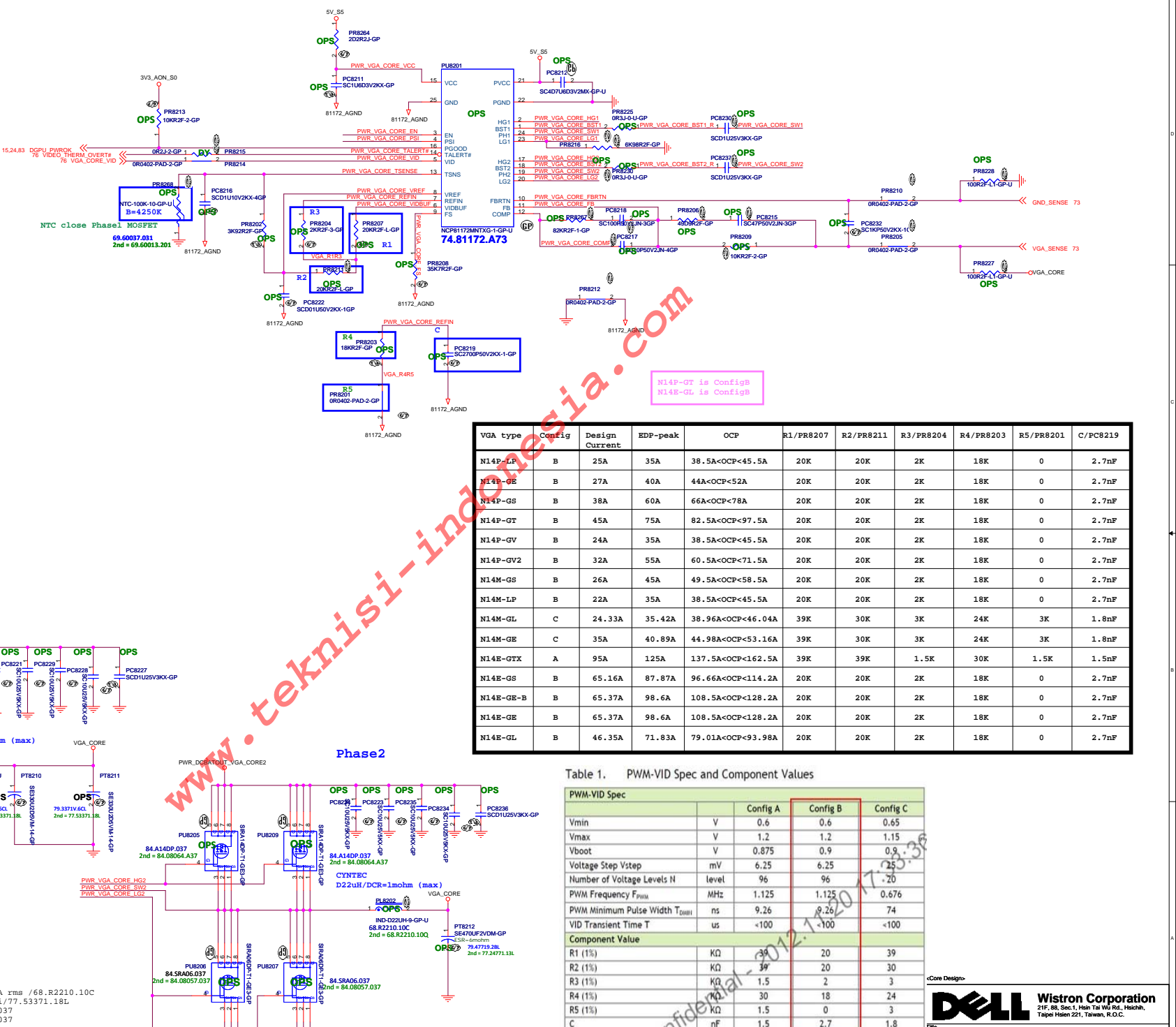
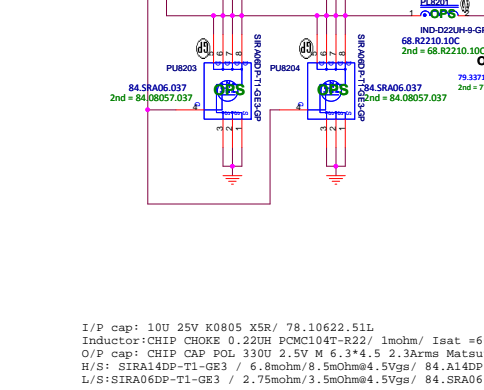
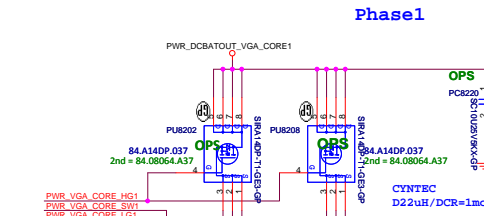
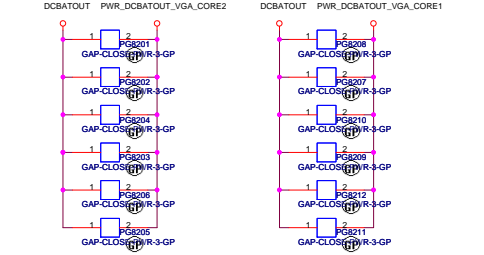
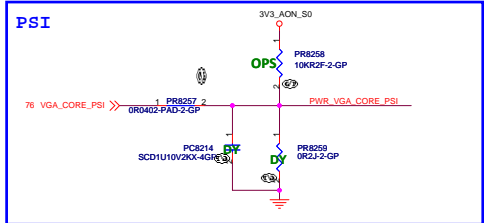
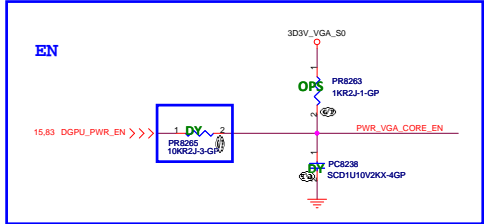
FBVREF Termination

Type	FBVREF%	Voltage	GPU GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low





SSID = GPU.Regulator



VGA type	Config	Design Current	EDP-peak	OCF	R1/PR8207	R2/PR8211	R3/PR8204	R4/PR8203	R5/PR8201	C/PC8219
N14P-LP	B	25A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GE	B	27A	40A	44A<OCP<52A	20K	20K	2K	18K	0	2.7nF
N14P-GS	B	38A	60A	66A<OCP<78A	20K	20K	2K	18K	0	2.7nF
N14P-GT	B	45A	75A	82.5A<OCP<97.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV	B	24A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV2	B	32A	55A	60.5A<OCP<71.5A	20K	20K	2K	18K	0	2.7nF
N14M-GS	B	26A	45A	49.5A<OCP<58.5A	20K	20K	2K	18K	0	2.7nF
N14M-LP	B	22A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14M-GL	C	24.33A	35.42A	38.96A<OCP<46.04A	39K	30K	3K	24K	3K	1.8nF
N14M-GE	C	35A	40.89A	44.98A<OCP<53.16A	39K	30K	3K	24K	3K	1.8nF
N14E-GTX	A	95A	125A	137.5A<OCP<162.5A	39K	39K	1.5K	30K	1.5K	1.5nF
N14E-GS	B	65.16A	87.87A	96.66A<OCP<114.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE-B	B	65.37A	98.6A	108.5A<OCP<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE	B	65.37A	98.6A	108.5A<OCP<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GL	B	46.35A	71.83A	79.01A<OCP<93.98A	20K	20K	2K	18K	0	2.7nF

Table 1. PWM-VID Spec and Component Values

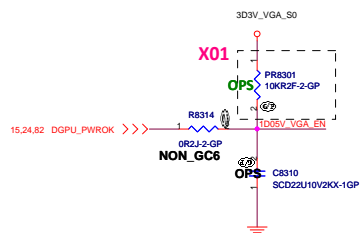
PWM-VID Spec	Config A	Config B	Config C
Vmin	0.6	0.6	0.65
Vmax	1.2	1.2	1.15
Vboot	0.875	0.9	0.9
Voltage Step Vstep	6.25	6.25	25
Number of Voltage Levels N	96	96	20
PWM Frequency F _{PWM}	1.125	1.125	0.676
PWM Minimum Pulse Width T _{PWM}	9.26	9.26	74
VID Transient Time T	us	<100	<100
Component Value			
R1 (1%)	KΩ	20	39
R2 (1%)	KΩ	20	30
R3 (1%)	KΩ	1.5	2
R4 (1%)	KΩ	30	18
R5 (1%)	KΩ	1.5	0
C	nF	1.5	2.7

```
SSID = PWR.Plane.Regulator
```

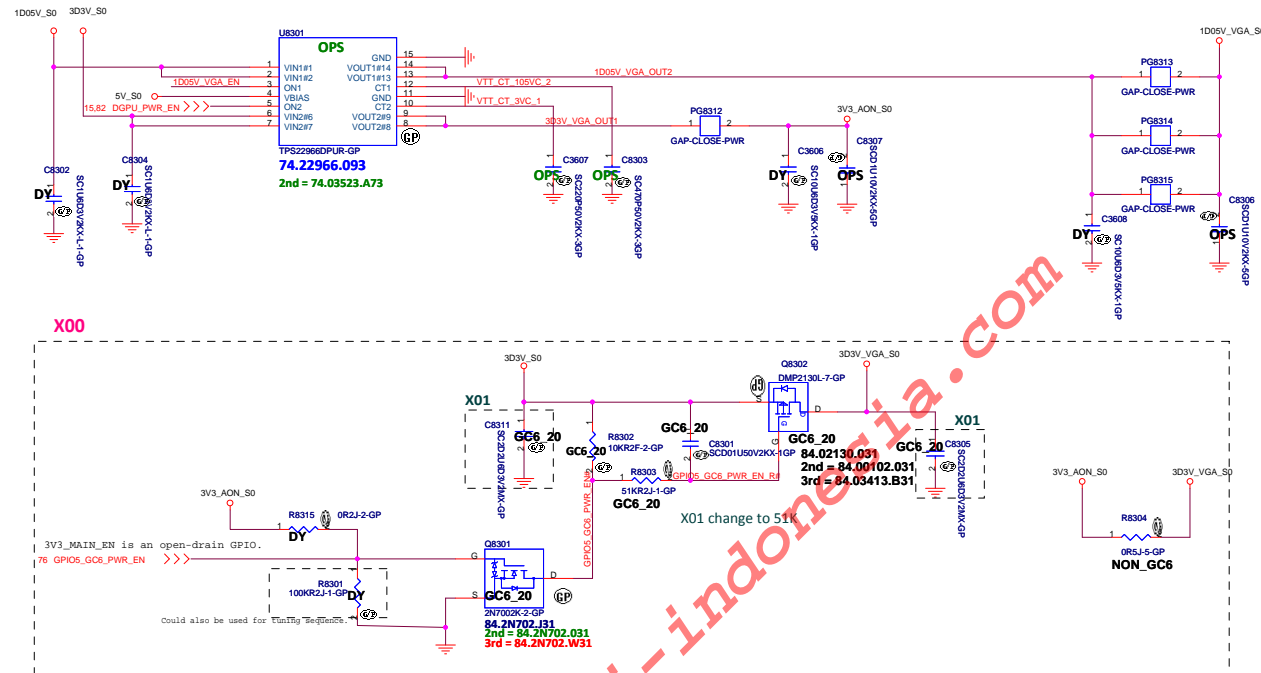
3D3V_VGA_S0

1D05V_VGA_S0

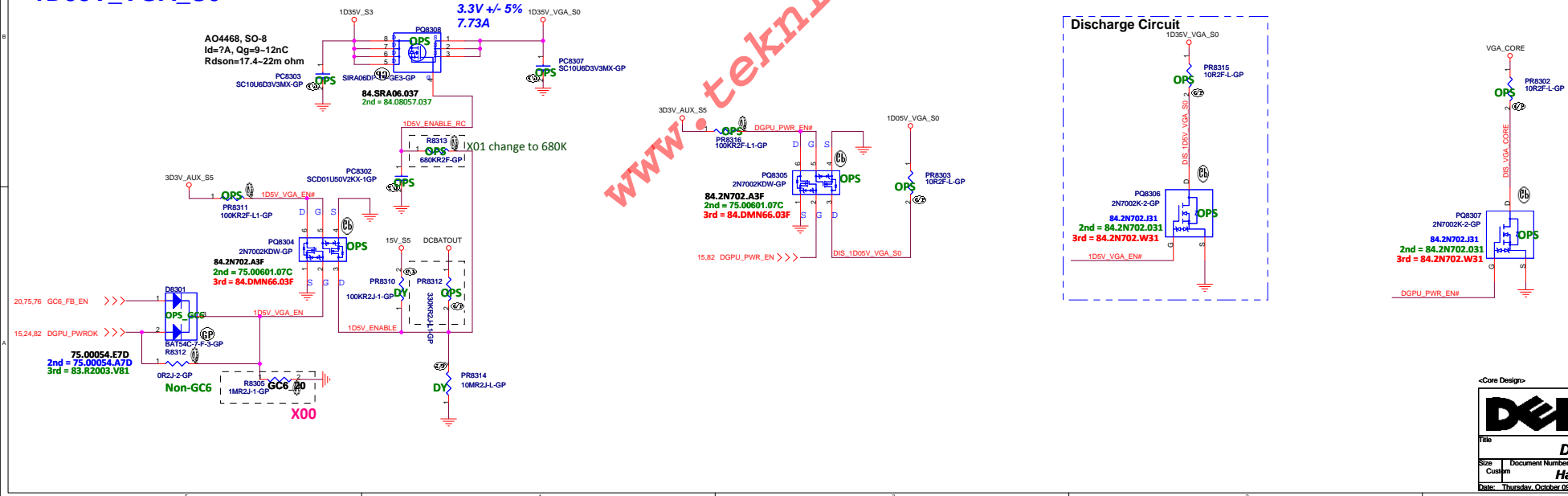
```
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0
```



```
3D3V_S0    to 3D3V_VGA_S0
1D05V_S0   to 1D05V_VGA_S0
```



1D35V_VGA_S0



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DIS VGA PWR			
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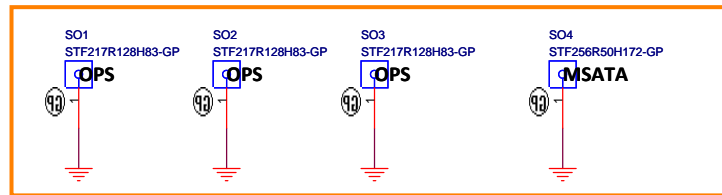
<Core Design>



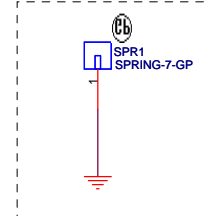
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Title			Reserved		
Size	Document Number				Rev
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SSID = User.Interface

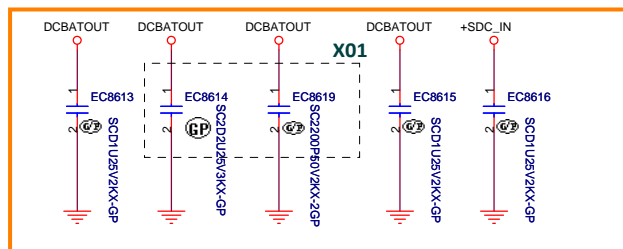
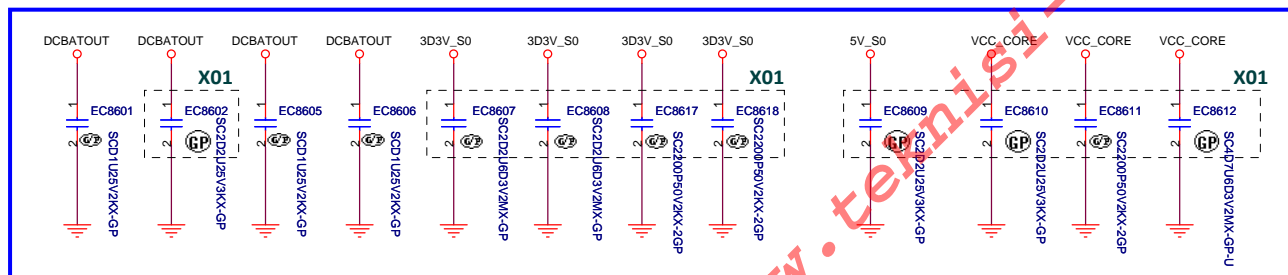
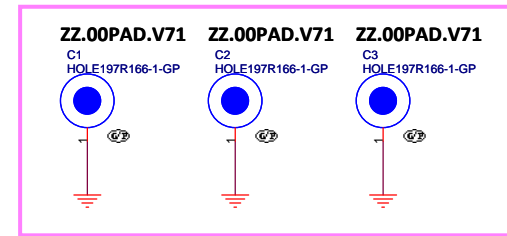
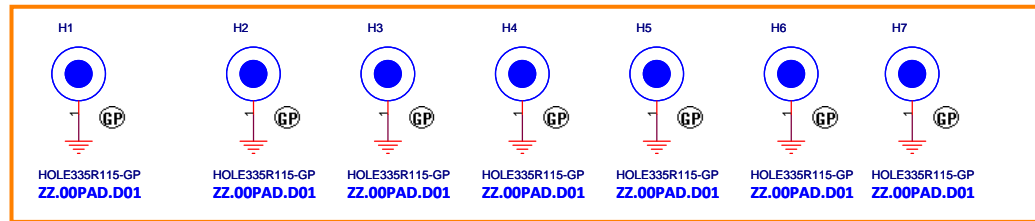


X02 0702 add



34.49U26.001

2nd = 34.43E28.001



<Core Design>




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Reserved		
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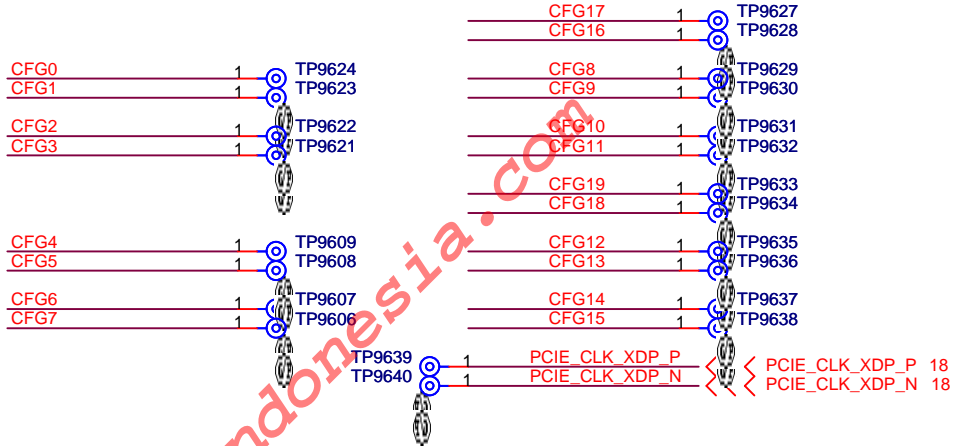
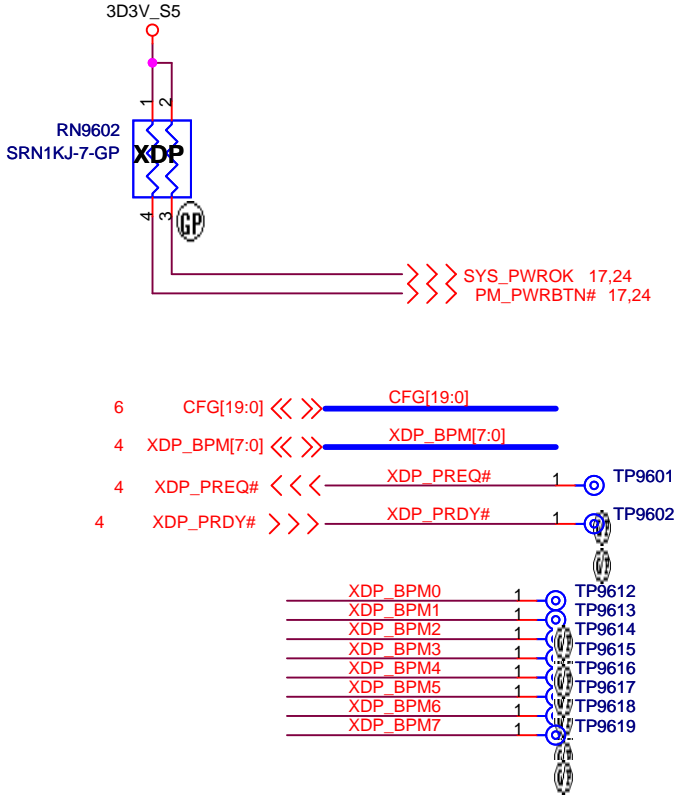
A00

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SSID = XDP

CPU XDP



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Title CPU XDP			
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Change History

3/17/2014

Change R2404 to 20K.
Add E51_TxD from KBC pin111(GPIO83) to wlan connector pin44. (Add R5805 00hm,DY)
Change TR3404,TR3405,TR3406,TR3407 source to 68.00201.311.Change R3404,R3405,R3406,R3407,R3423,R3424,R3415,R3441 form 0402 to 0603. (00hm).
Dummy R2437, R2441, C2419, C2420.
Change R8303 from 0K to 51K.
Change R8313 from 0K to 680K.

3/20/2014

Add C3513,C3514(Dummy).
Dummy D2401, add R2448; Change USB_DET# pull high power rail to 3D3V_AUX_S5.

3/23/2014

Stuff R6215, R2447.

3/25/2014

Change PR4516 to 16K. PR4518 to 10.2K.

3/27/2014

Change PR4626 from 100K to 150K.Change PR4610 to 422K. PR4620 to 3.9K.
Stuff TR3404,TR3405,TR3406,TR3407. Dummy co-lay resistor.
Change PT4501, PT4502 source to 79.22710.3KL. Add second source 77.52271.09L.

3/28/2014

Add and stuff TR6301,TR6302 (3/25 removed). Dummy co-lay resistor.

3/29/2014

Add PC4435, PC4436, PC4437(dummy), PC4438(dummy).
Delete AFTP3402,AFTP3403.
Add D2001,R2030. Delete R1512.
Stuff R2444, Dummy R6203
Change INT_TP#_GPIO55 pull high power rail to 3D3V_S0.

3/31/2014

Add EC8617, EC8618, EC8619,PC4609.(2200pF)
Change EC4601,EC8608,EC8607,C1203,PC4901,EC8614,C8311,C8305,EC8602,EC8609,EC8610,C2501,C1310 to 2.2u, EC8611,PC5103,PC5126 to 2200P.

4/14/2014

Change PR8263 to 1K, PR8301 to 10K, C8310 to 0.22u.

9/9/2014

Change PN2008 to 2.2K

10/8/2014

Add C1217(DUMMY),C1319(DUMMY),D2002(DUMMY)

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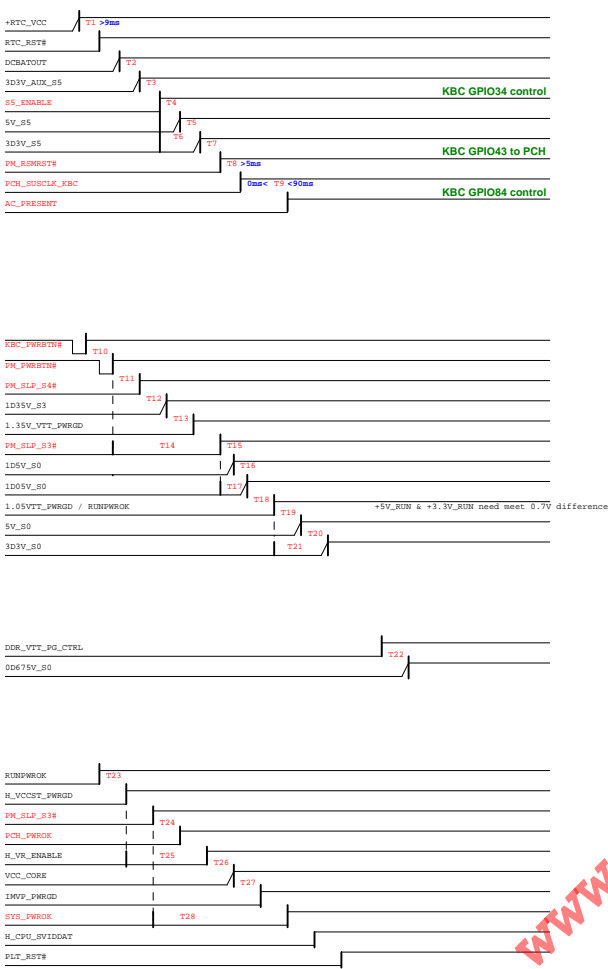
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Intel-Power Up Sequence

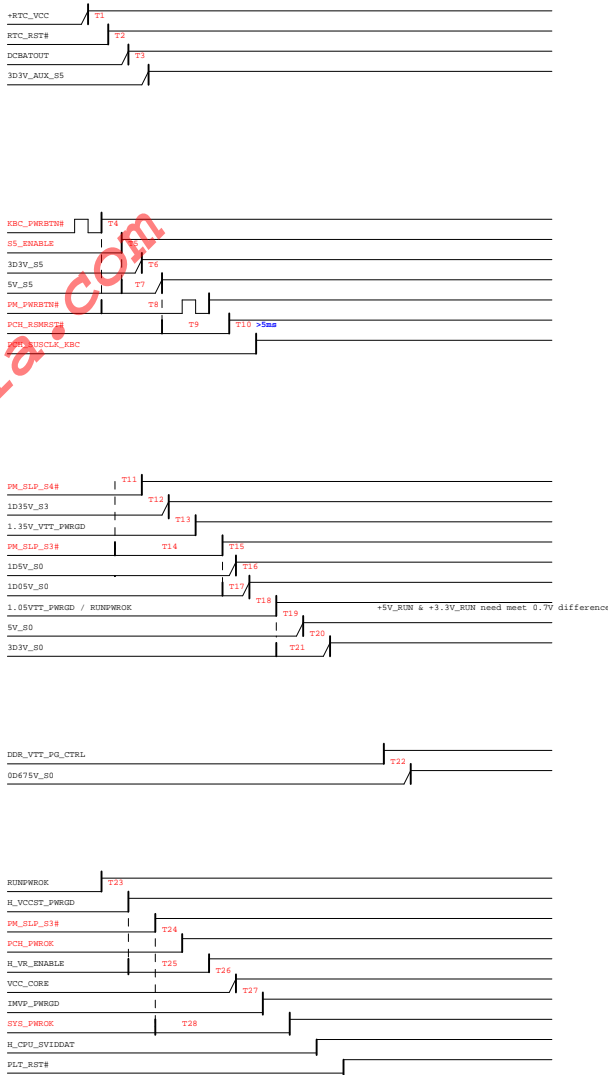
(AC mode)

Red printings:KBC GPIO involved

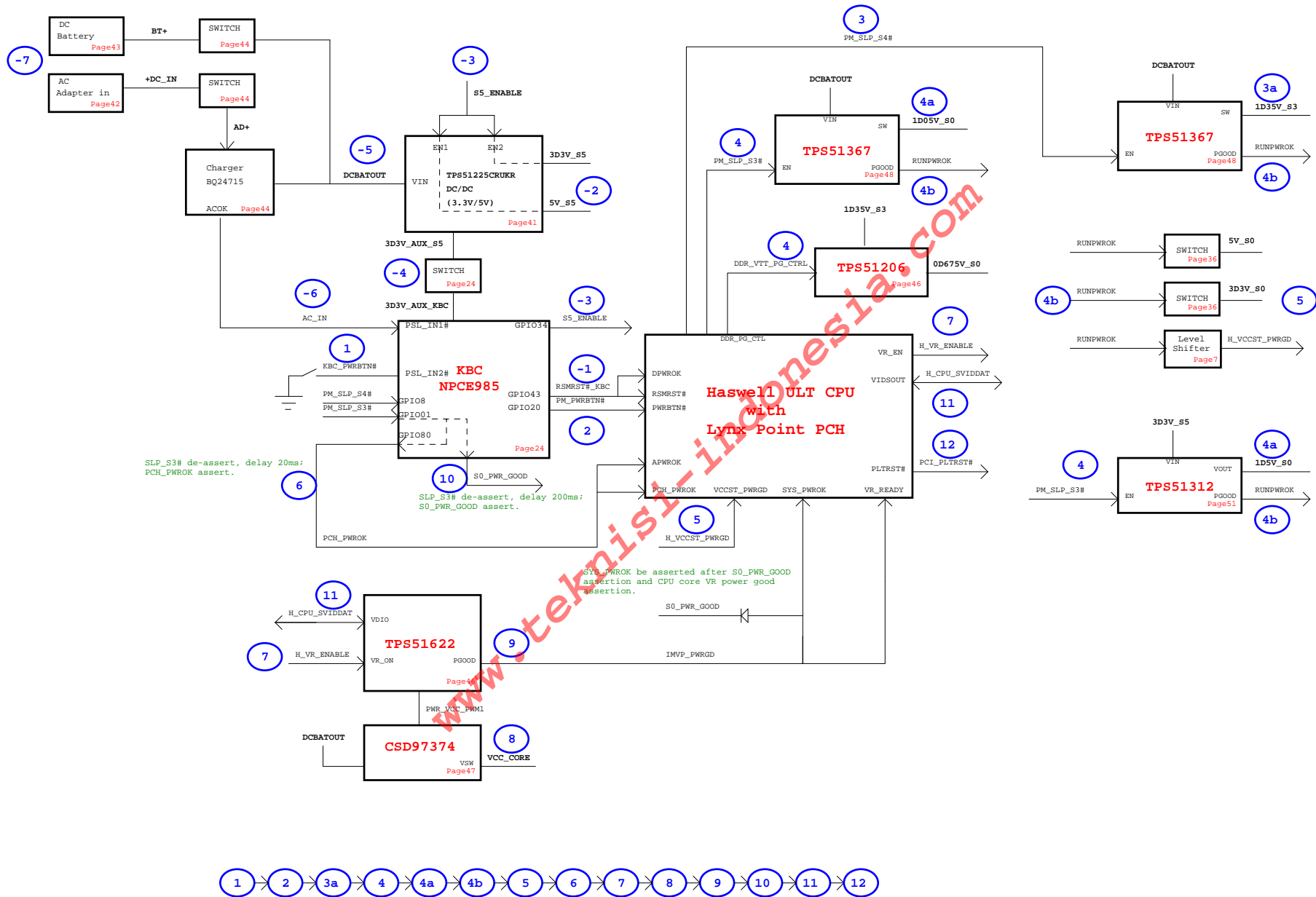


(DC mode)

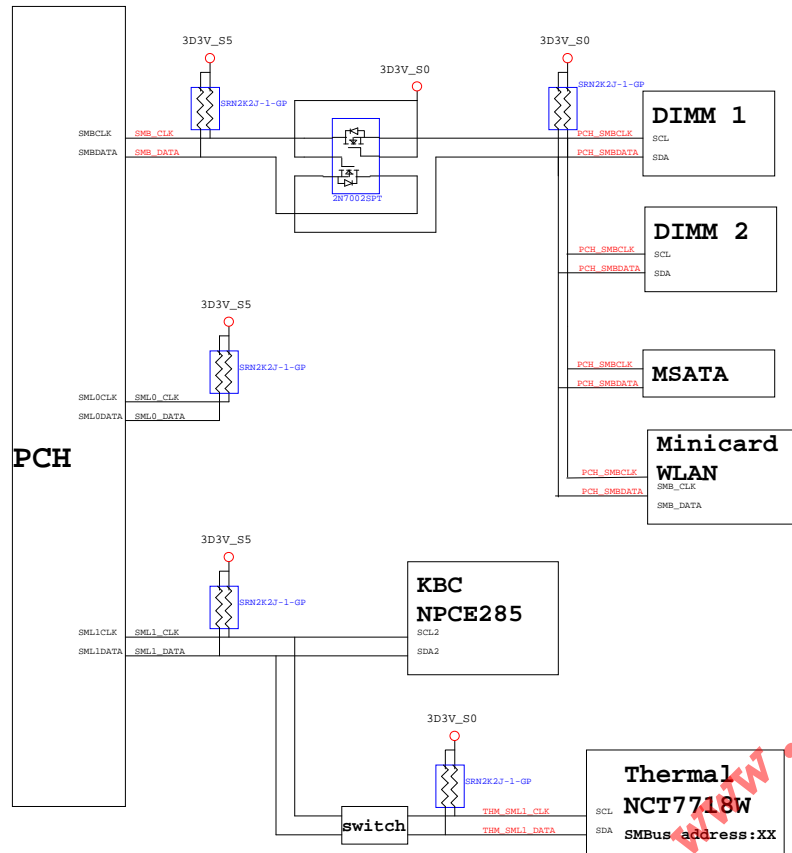
Red printings:KBC GPIO involved



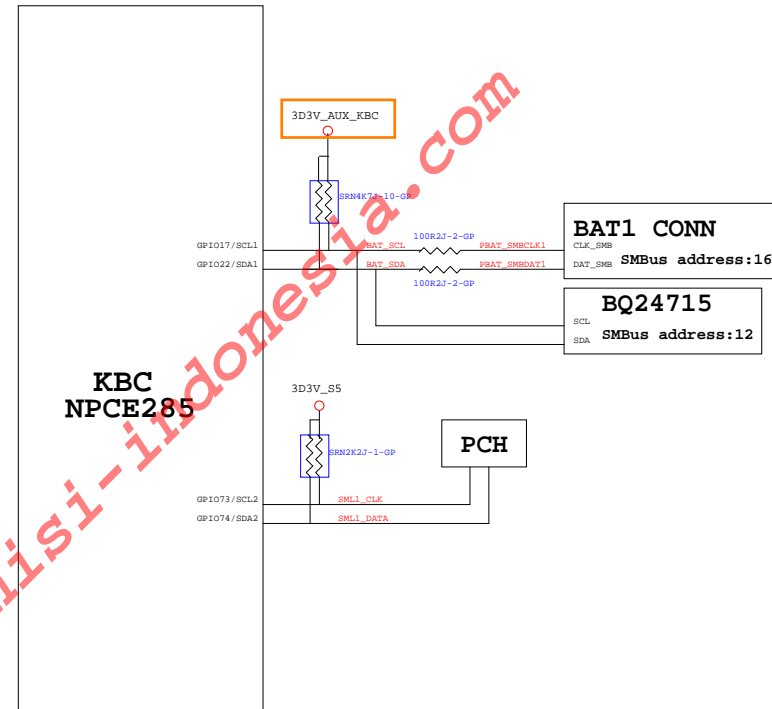
Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



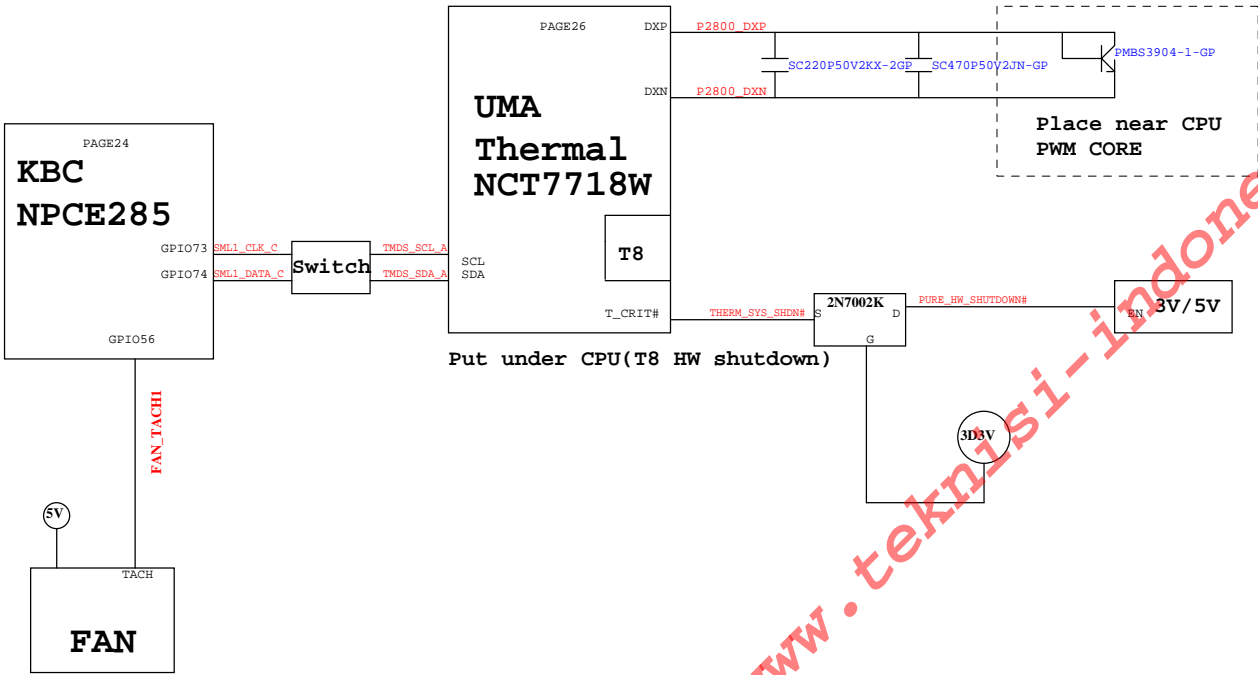
PCH SMBus Block Diagram



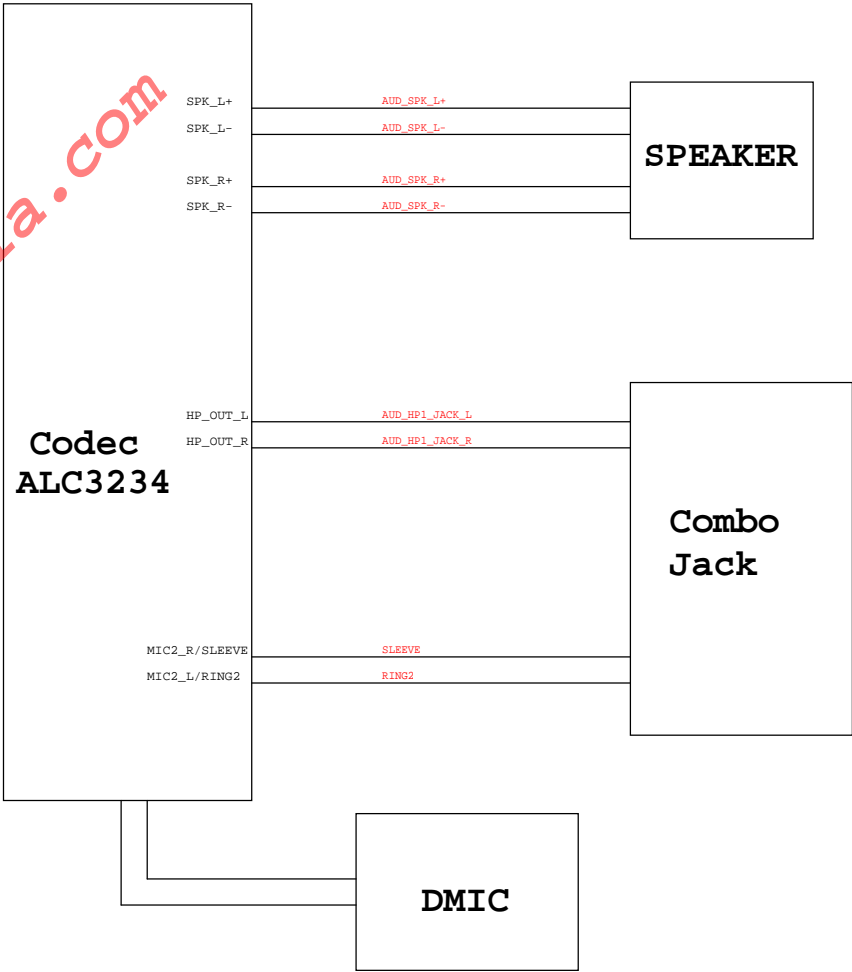
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



CLK Block Diagram

